Backside Via Process with Defect Free Sidewalls for GaN MMIC Applications

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Abstract

Backside via etch process for GaN on SiC devices was studied. Etch condition has been optimized to suppress the formation of undesirable pillars and post etch cleaning processes were applied to ensure the etch byproducts of SiC substrate and AlGaN/GaN epi layers are completely removed. Through carefully designed test steps we were able to develop a 70um diameter backside via process with defect free side walls which is critical for fabricating reliable GaN based MMICs.

INTRODUCTION

GaN on SiC based high electron mobility transistors (HEMTs) have been popular candidates for RF, high-power, low noise, and high-temperature applications due to their outstanding material properties [1,2]. To improve its performances and reliability backside vias can be applied, however forming backside vias is challenging due to SiC substrates being extremely stable that they require high power inductively coupled plasma (ICP) with proper mask layer to be etched with reasonable etch rate [3,4]. Suppressing and removing etch byproducts is also important because the circuits on the front sides are electrically connected to the ground on the backside through metallized side walls of the vias where the etch byproducts stick [5]. In this paper, we present a 70um diameter backside via process with defect free side walls. Ni etch mask was used to ensure high selectivity to SiC and short descum step was applied before etching to prevent the formation of pillars. After etching was complete etch byproducts were removed by ultrasonic cleaning in an acidic solution.

EXPERIMENT

The GaN on SiC wafer with completed front side processes was bonded with SiC carrier wafer using wafer bonder from Brewer Science, Inc. Choosing the right bonding material that does not cause contamination and remains stable under high temperature is critical because etching SiC substrate requires high energy plasma which causes the temperature of the wafer to rise during the process. Then the backside of the GaN on SiC wafer was thinned to 100um through a lapping process.

After the lapping process, vias with 70um diameter were patterned, Ti/Au with thickness of 50/100Å was deposited as a base metal layer and Ni with thickness of >4um was electroplated as an etch mask. Ni is selected for the etch mask due to high etch selectivity to SiC in the range of 30~40:1 [6]. Depositing base metal after photolithography has an advantage over the other way around because the base metal is not etched during the etching process therefore reduces the chance of forming pillars. This method however has a potential risk of having Ni plated on the sidewall and the top of the photoresist but can be avoided by optimizing the photolithography process.

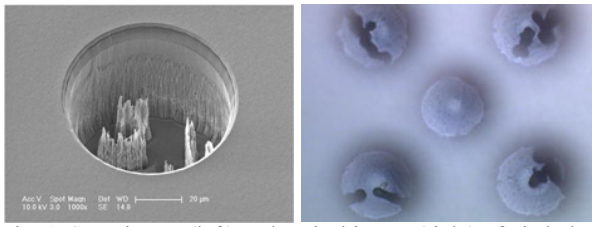

Fig. 1. SEM image (left) and optical image (right) of via holes without descum process.

The surface of SiC was cleaned with descum step to remove defects which causes pillars during the etching process. Because the pillar formation in SiC via holes is attributed to a process in which the origin of micropipes acts as a micromask and is passivated with nonvolatile products generated by a chemical combination of the etched Ni from the metal mask and the formed SiF_X species during etching, the surface treatment by descum process can significantly reduce the formation of pillars [7]. A via hole without descum is shown in Figure 1.

After descum process step, the SiC substrate was etched with SF_6 based plasma with the rate of 1.9um/min. Etching SiC produces a large amount of etch byproducts formed on the side walls of the vias and some of the byproducts fall onto the bottom of the vias. These byproducts as shown in Figure

2 can be removed by ultrasonic cleaning using diluted hydrochloric acid as a cleaning solvent.

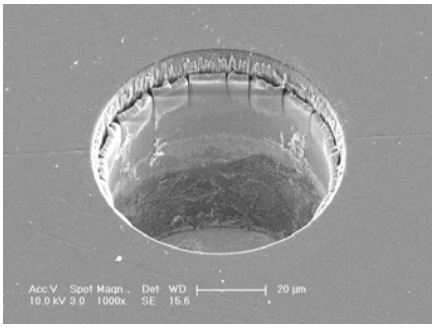

Fig. 2. SEM image of via hole before ultrasonic cleaning.

The effect of ultrasonic cleaning is shown in Figure 3. After the Ni mask and underlying base metal was removed, the GaN epi layer was etched by Cl_2 based plasma. Both SiC and GaN etch processes were carried out by SPTS. The etch byproducts can be removed through ultrasonic cleaning with DI water instead of acidic solution in order to prevent damaging metal pads (etch stop layer) on the front of the wafer. The effect of ultrasonic cleaning is shown in Figure 4.

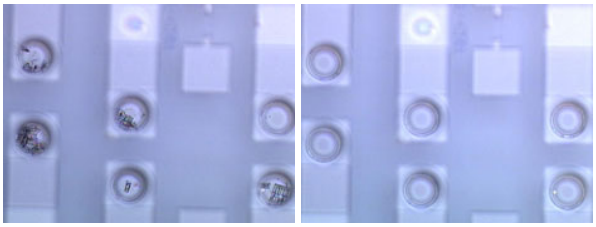

Fig. 3. Optical image of via hole before (left) and after (right) ultrasonic cleaning (after SiC etching).

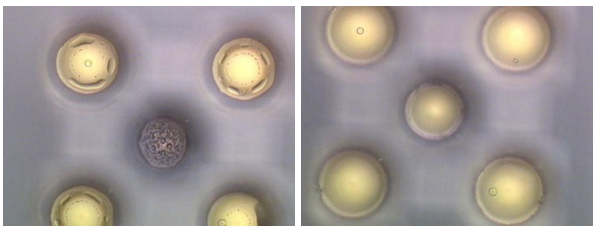

Fig. 4. Optical image of via hole before (left) and after (right) ultrasonic cleaning (after GaN etching).

It is shown in Figure 5 that the via is virtually defect free and has a very smooth sidewall. Such cleaning process for removing etch byproduct on the sidewall is crucial for monolithic microwave integrated circuit (MMIC) fabrication because it directly affects the connectivity of vias when they are electroplated. After the etching is complete a base metal layer was then deposited and Au with thickness of 5um was electroplated. SEM image of electroplated via hole is shown in Figure 6. Photograph of a X-band GaN MMIC with backside vias fabricated through the processes described above is shown in Figure 7.

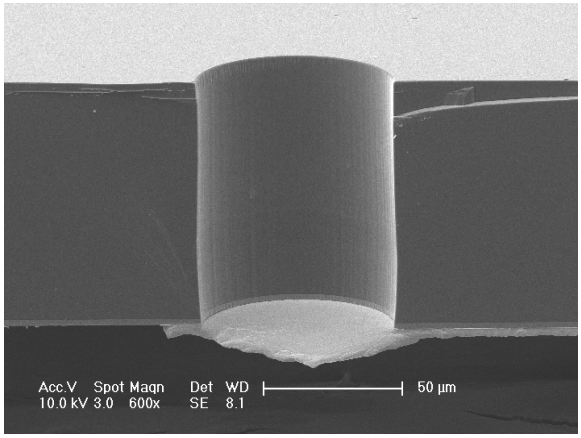

Fig. 5. SEM image of via hole prior to metallization.

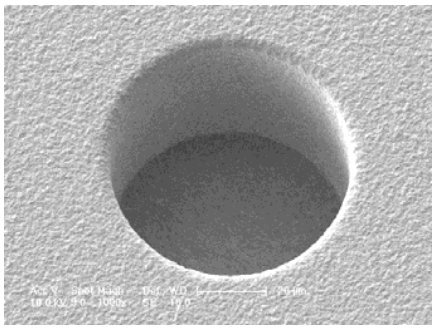

Fig. 6. SEM image of via hole after metallization.

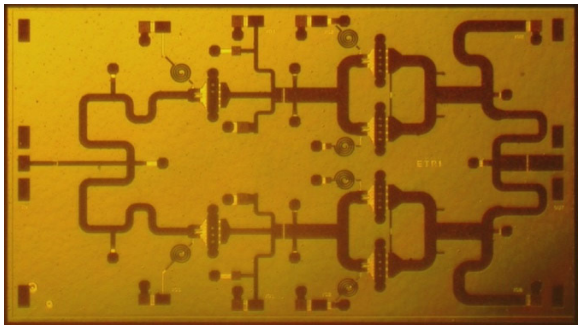

Fig. 7. Photograph of a X-band GaN MMIC.

CONCLUSIONS

Fabrication process of backside via on GaN on SiC devices was demonstrated. Via patterning before base metal deposition along with descum successfully suppressed the formation of pillars during SiC etching and resulted in a very smooth side wall. Post etch treatment using ultrasonic was proven to be very effective in removing etch byproducts without damaging the etch stop layer.

ACKNOWLEDGEMENTS

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REFERENCES

[1] Mishra, Umesh K., Primit Parikh, and Yi-Feng Wu. "AlGaN/GaN HEMTs-an overview of device operation and applications." Proceedings of the IEEE 90.6 (2002): 1022-1031.

[2] Yoon, Hyung Sup, et al. "Microwave Low-Noise Performance of 0.17um Gate-Length AlGaN/GaN HEMTs on SiC With Wide Head Double-Deck T-Shaped Gate." IEEE Electron Device Letters 37.11 (2016): 1407-1410.

[3] Stieglauer, H., et al. "Evaluation of through wafer via holes in SiC substrates for GaN HEMT technology." CS MANTECH Conference, 2012.

[4] Fan, Frank, et al. "Qualification of Backside Via Etch Process in GaN-on-SiC HEMT Devices." CS MANTECH Conference, 2015.

[5] Chen, Chia-Hao, et al. "Method for Forming Through Wafer Vias in GaN on SiC Devices and Circuits." CS MANTECH Conference, 2014.

[6] Barker, Anthony, et al. "Advances in Back-side Via Etching of SiC for GaN Device Applications." CS MANTECH Conference, 2013.

[7] Okamoto, Naoya. "Elimination of pillar associated with micropipe of SiC in high-rate inductively coupled plasma etching." Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films 27.2 (2009): 295-300.

ACRONYMS

HEMT: High Electron Mobility Transistors
MMIC: Monolithic Microwave Integrated Circuit
ICP: Inductively Coupled Plasma