Some Process Development Issues for Ka-band GaN HEMT Individual Source Via (ISV)

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Abstract

In this paper we report on the development of individual source vias (ISV) for Ka-band GaN HEMT technology. By addressing some key process issues, we have successfully developed ISV and integrated it into our Ka-band device technology. The results indicate that GaN HEMTs integrated with ISV effectively reduce source inductance and improves device RF performance.

INTRODUCTION

GaN HEMT devices have been developed for their potential applications in high frequency and high power applications. With GaN devices moving into higher frequencies, gate length has been reduced, such as 0.15 µm gate process has been developed for Ka band [1-2]. Reducing gate length also increases device gain. Devices gain can also be improved by reducing source inductance. The maximum frequency of Ka-band devices can be increased by adding more vias and arranging via layout [3].

In this paper, we report on the development and integration of the ISV process into Qorvo's 100-mm 0.15-µm GaN process. We demonstrate the reduction of source inductance and its effect on device performance.

INDIVIDUAL SOURCE VIA DEVELOPMENT AND INTEGRATION

To realize ISV process, the via size has to be small enough to fit onto the source pad, where the maximum size is limited by delay time considerations. As the via aspect ratio increases, the via etch rate drops making the process more challenging. Smaller ISV also causes other integration challenges such as alignment of the via to frontside and via plating, which are the focus of this report. We have studied vias with different shapes and sizes and via area ranges around 700 µm^2 to 1200 µm^2. For the discussion below, all the results are from 30 µm x 30 µm ISV.

In order to facilitate the via etch process, via size has to be as large as possible. To maximize via size, we have to reduce misalignment from backside to frontside. However, aligning back to front is challenging as we are aligning two layers that are 100 µm apart. We have developed a new alignment scheme which reduces the misalignment from as high as 7 µm to less than 4 µm as shown in Fig. 1.

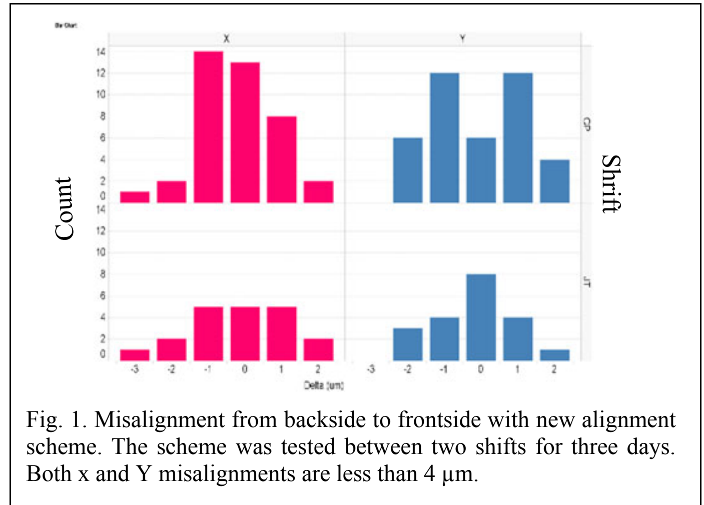

Fig. 1. Misalignment from backside to frontside with new alignment scheme. The scheme was tested between two shifts for three days. Both x and Y misalignments are less than 4 µm.

The second challenge is that via plating steps for the non-ISV process of record give low yields. Table I and Fig. 2 show the via yield as mapped from electrical tests. Yields less than 50% with rough via side walls and nodules are observed with the process of record in the vias even though the via do make good electric contact to frontside metal pad. The causes are identified as related to via plating integration steps, such as cleaning and pre-wet. A new process is developed and the via yield increases to over 90% with un-yielded vias around wafer edge, which are presumably due to via etch. As shown in Fig. 3, smoother plating is achieved with new ISV integration process. Not discussed here, but further improvement on via plating process has improved via plating efficiency with Au via bottom to top field Au thickness ratio increases from 0.60 to 0.89.

TABLE I.
VIA CONTINUITY YIELD FOR LARGE VIA AND ISV INTEGRATION PROCESSES.

Old integrated process		**ISV integrated process**	
Wafer No	Via continuity yield	Wafer No	Via continuity yield
1	27.3%	1	87.7%
2	44.3%	2	96.5%
3	46.6%	3	99.1%
		4	95.6%

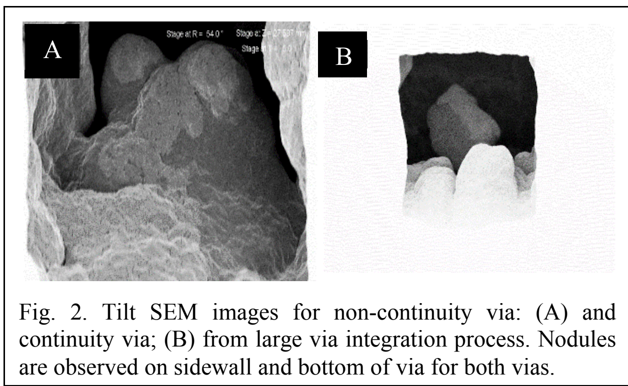

Fig. 2. Tilt SEM images for non-continuity via: (A) and continuity via; (B) from large via integration process. Nodules are observed on sidewall and bottom of via for both vias.

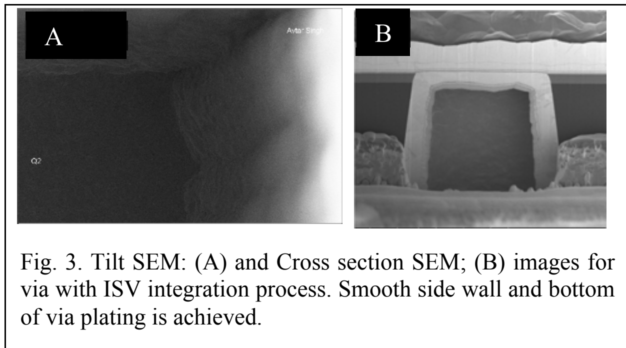

Fig. 3. Tilt SEM: (A) and Cross section SEM; (B) images for via with ISV integration process. Smooth side wall and bottom of via plating is achieved.

DEVICE PERFORMANCE EVALUATION

0.15 µm GaN HEMT devices fabricated with Qorvo's 3MI technology are used as test vehicle to evaluate the effect of ISV on device RF performance. Devices with ISV and end vias (EVIA) are fabricated side by side and evaluated. The small signal performance is examined by using 4x100 µm transistor while large signal performance is examined by 4x50 µm transistor (Fig. 4).

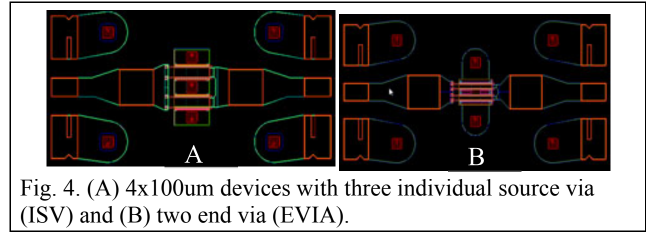

Fig. 4. (A) 4x100um devices with three individual source via (ISV) and (B) two end via (EVIA).

Fig. 5. shows the source inductance extracted from small-signal S-parameter measurements on both ISV and EVIA 4x100 µm transistors. As expected, devices with ISV have smaller source inductance (Ls): median Ls of 0.099nH compared to 0.0145 nH for devices with EVIA. The lower source inductance from ISV transistors indicates that they have better RF grounding than EVIA transistor construction. It results in higher extrinsic stable gain for ISV transistor.

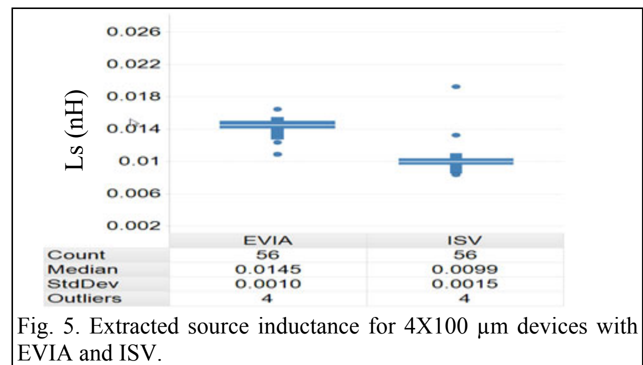

Fig. 5. Extracted source inductance for 4X100 µm devices with EVIA and ISV.

The improved RF performance with ISV devices is shown on small-signal performance. As shown in Fig. 6, device with ISV demonstrates higher maximum stable gain and maximum available gain than EVIA devices. The devices with ISV also increase the MAG/MSG turning point by 2 GHz, which is contributed from its lower source inductance. The actual Fmax increases more than 10 GHz.

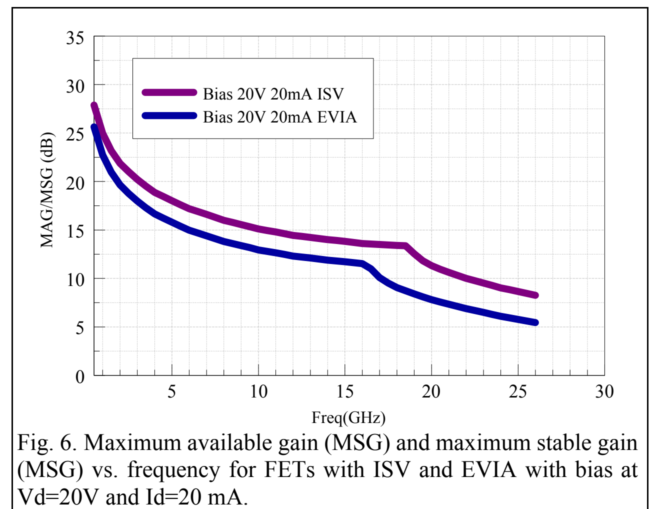

Fig. 6. Maximum available gain (MSG) and maximum stable gain (MSG) vs. frequency for FETs with ISV and EVIA with bias at Vd=20V and Id=20 mA.

The large-signal performance of both devices with ISV and EVIA are characterized using 30 GHz load-pull test. Under Vd=20V and Id=20 mA (100 mA/mm) bias condition and with the same efficiency load-pull tuning approach, ISV device achieves peak PAE (Power Added Efficiency) of 47%, Pout of 28 dBm (3.15 W/mm) and gain of 7.9 dB. Pout, gain and PAE vs. Pin is plotted in Fig. 7. However, the EVIA device shows peak PAE of 45.9%, Pout of 27.9 dBm (3.08 W/mm) and power gain of 7.4 dB. Clearly the ISV device demonstrates a better power performance than EVIA device in terms of PAE and power gain at Ka-band.

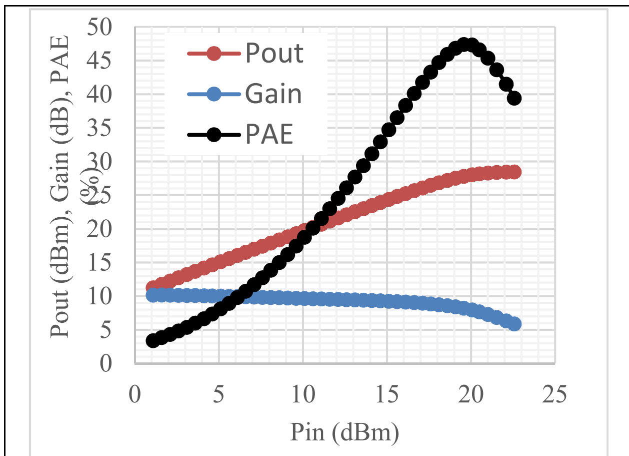

Fig. 7. Loadpull measurement of 4x50 µm FET with ISV at 30 GHz, biased at Vd=20V, Id =20 mA and tuned at maximum efficiency.

Conclusion

We have demonstrated individual source via technology, which is successfully incorporated into Ka band GaN HEMT devices configuration. As expected, individual source via reduced source inductance and increase maximum stable gain and frequency for maximum stable gain. Meanwhile, ISV device demonstrated a better power performance than EVIA device at Ka-band.

Acknowledgements

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Acronyms

ISV: Individual Source Vias
HEMT: High Electron Mobility Transistor
Fmax: Maximum Frequency of Oscillation
EVIA: End Vias