

Thick (6 μm) n-type GaN-on-Si Epi-Layers for Vertical Power Devices

L. Zhang, P. Xiang, K. Liu, H. Huo, H. Ding, N. Yin, and K. Cheng*

Enkris Semiconductor, Inc., Room 517A, NW-20, 99 Jinji Lake Avenue, Suzhou Industrial Park, 215123, P. R. China

* e-mail: chengk@enkris.com, Phone: +86-0512-6270-6800

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Abstract

We demonstrate the growth of high quality n-type GaN on large scale Si substrates in the push towards commercialization of vertical power devices. Around 6 μm thick crack-free GaN layer was achieved by metal organic chemical vapor deposition. The GaN growth rate is faster than 4 $\mu\text{m}/\text{hr}$, offering significant growth time savings and faster manufacturing process throughput. The average root mean square surface roughness is less than 0.2 nm. Carrier mobility is as high as 719 cm^2/Vs with n-type dopants of $< 3\text{E}16/\text{cm}^3$. The threading dislocation density is estimated to be $< 2.5 \times 10^8 \text{ cm}^{-2}$ for growth on both 150 mm and 200 mm Si substrates. These results satisfy the growth requirements for processing GaN based high-power devices and thus suggest that GaN-on-Si technology has great potential to achieve cost-effective GaN devices, which are industries desired.

INTRODUCTION

Goup-III nitrides are promising materials thanks to the excellent performance in a variety of optical and electronic devices. Among GaN-based high-power devices, conventional lateral structure, such as high-electron-mobility transistors (HEMT), have been studied extensively. These lateral devices are typically rated at 600-650V, and have recently become commercially available.

Recently, vertical power devices have been demonstrated [1-3]. The first vertical structure with excellent performance was reported on bulk GaN substrates [1]. Quasi-vertical and fully vertical diodes on Si substrates have also been developed [2, 3]. A breakdown voltage of higher than 300 V was achieved with 1.5 μm thick GaN layers grown on Si substrates.

Although vertical devices are promising for high power applications, they have not yet been produced on a commercial level. To meet the demand for 600 V voltage devices, several epitaxy requirements need to be fulfilled. Firstly, GaN epilayers should be fabricated at a competitive cost. Secondly, according to the fundamental figure of merit (FOM) parameters for GaN, GaN drift layer thickness should be at least 6 μm and the net donor doping density should be lower than $5 \times 10^{16} \text{ cm}^{-3}$ [4]. Furthermore, dislocation density

should be as low as possible, and GaN surface should be as smooth as possible. These all can help improve breakdown voltage and reduce leakage current.

In this report, high-quality GaN epilayers grown on 150 / 200 mm Si substrates are demonstrated. By using Enkris unique GaN-on-Si technology, around 6 μm thick GaN epilayer was achieved in a single continues growth with only a $\sim 600 \text{ nm}$ thin buffer layer. The threading dislocation density (TDD) of GaN epilayer is around $< 2.5 \times 10^8 \text{ cm}^{-2}$ and average root mean square (RMS) roughness is less than 0.2 nm. Carrier mobility is as high as 719 cm^2/Vs . These economic and high quality GaN wafers are a key step toward the commercialization of vertical GaN devices.

RESULTS AND DISCUSSION

All wafers were grown on 150 / 200 mm Si (111) substrates by metal organic chemical vapor deposition (MOCVD) in a multi-wafer reactor. The discussions are mainly focused on 6 inch wafers. Trimethylgallium (TMGa), trimethylaluminium (TMAI) and ammonia (NH_3) are used as the precursors, and silane (SiH_4) as the n-type dopants.

The GaN epilayer was fabricated in a single continuous growth without any interlayers. The GaN thickness was confirmed by the scanning electron micrograph (SEM) measurements. As shown in Fig. 1, around 6 μm thick GaN was achieved on Si substrate with only a 600 nm thin buffer layer. The GaN growth rate is faster than 4 $\mu\text{m}/\text{hr}$, offering significant growth time savings and faster manufacturing process throughput.

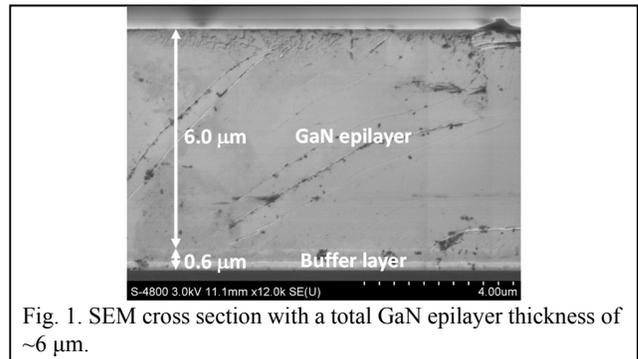


Fig. 1. SEM cross section with a total GaN epilayer thickness of $\sim 6 \mu\text{m}$.

Surface morphology is an important factor as a rough surface would increase leakage current due to larger local electrical field at the surface peak [5]. The average RMS roughness across a $5\ \mu\text{m} \times 5\ \mu\text{m}$ scanned GaN surface area is only 0.18 nm.

Both thickness and bow map of 150 mm GaN-on-Si wafers are shown in Fig. 2. This 6 inch wafer is very flat with bow map of $-16\ \mu\text{m}$, and the average thickness is $\sim 6.6\ \mu\text{m}$ with uniformity of 1.8%.

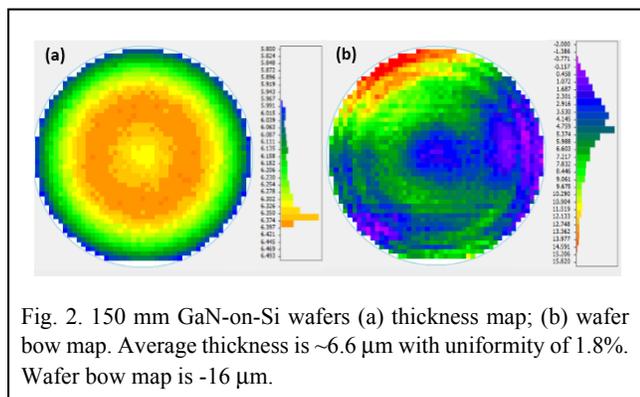


Fig. 2. 150 mm GaN-on-Si wafers (a) thickness map; (b) wafer bow map. Average thickness is $\sim 6.6\ \mu\text{m}$ with uniformity of 1.8%. Wafer bow map is $-16\ \mu\text{m}$.

It is important to grow thick GaN with desired Si doping concentrations. Fig. 3 shows in-situ wafer curvature measured during the growth of nGaN step with different doping concentrations. It has been reported that compressive stress can be easily relaxed via threading dislocation inclination in the presence of high density threading dislocations [6]. In this work, in situ curvature measurements show straight line with a constant slope even at Si-doping level of $>1\text{E}19/\text{cm}^3$, which indicates minimum compressive stress relaxation. This can be explained by the fact that high quality GaN with low TDD can be grown up to very thick layers due to the absence of compressive stress relaxation.

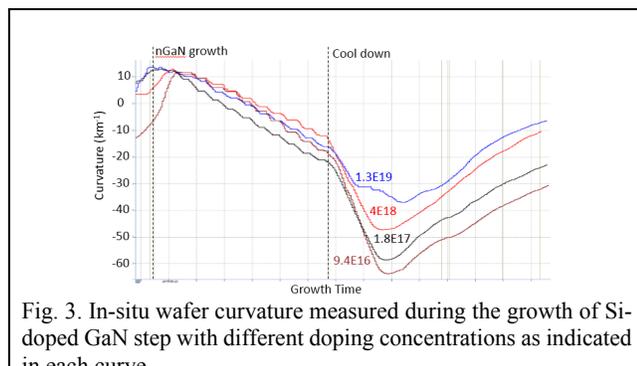


Fig. 3. In-situ wafer curvature measured during the growth of Si-doped GaN step with different doping concentrations as indicated in each curve.

The epi-layers have been characterized by XRD rocking curve (RC) scans. The full-width at half-maximum (FWHM) of RC (102) cross the whole 150 mm GaN-on-Si wafers is well controlled below 300 arcsec (Fig. 4). TDD was estimated

by cathodoluminescence (CL) measurements, and the TDD is estimated as to be $< 2.5 \times 10^8\ \text{cm}^{-2}$ for growth on both 150 mm and 200 mm Si substrates. The CL image of 200 mm GaN-on-Si is shown in Fig. 5.

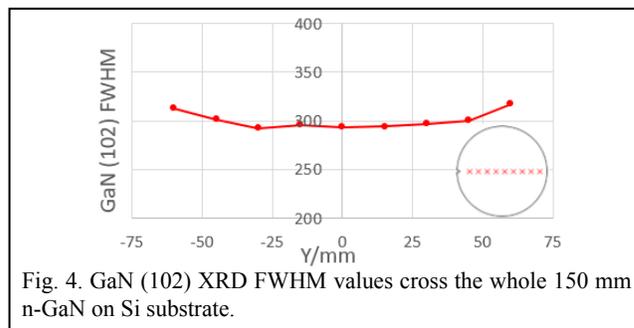


Fig. 4. GaN (102) XRD FWHM values cross the whole 150 mm n-GaN on Si substrate.

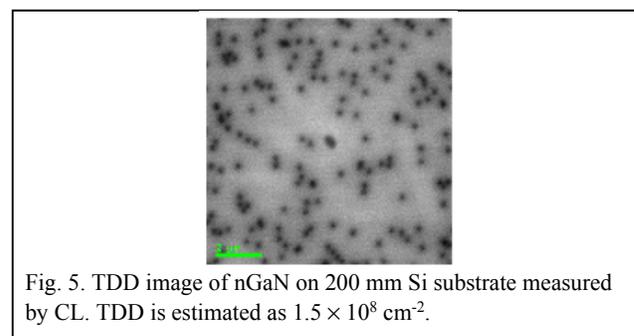


Fig. 5. TDD image of nGaN on 200 mm Si substrate measured by CL. TDD is estimated as $1.5 \times 10^8\ \text{cm}^{-2}$.

Higher mobility of GaN can further reduce the ON-resistance. Low-field electron mobility as a function of doping concentration in GaN at room temperature is shown in Fig. 6. It is observed that a moderate Si doping during the GaN growth improves the electron mobility and the electron mobility is higher for the nGaN-on-Si with optimized growth conditions. It has been reported that an increase in edge dislocations will cause the

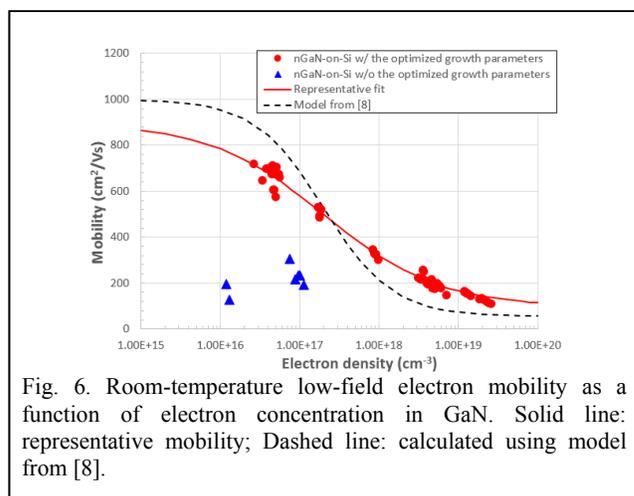


Fig. 6. Room-temperature low-field electron mobility as a function of electron concentration in GaN. Solid line: representative mobility; Dashed line: calculated using model from [8].

reduction of the electron mobility due to the influences of charged defects, which are from dangling bonds along the edge dislocation lines [7]. The best doping effects and the electron mobility strongly depends on the background impurity and dislocation density of the sample. Mobility as high as 719 cm²/Vs is achieved at doping concentration of < 3E16/cm³.

CONCLUSIONS

High quality GaN with low TDD grown on large scale substrates is demonstrated for vertical power structures. These results suggest a cost-effective solution for high performance vertical power devices.

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ACRONYMS

HEMT: High Electron Mobility Transistors
MOCVD: Metal Organic Chemical Vapor Deposition
TDD: Threading Dislocation Density
SEM: Scanning Electron Microscope
RC: Rocking Curve
FWHM: Full Width at Half Maximum
CL: Cathodoluminescence

