Low Leakage High Breakdown GaN MOSHEMTs on Si with a ZrO_2 Gate Dielectric

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Abstract

This paper reports on high voltage GaN metal-oxide-semiconductor high electron mobility transistors (MOSHEMTs) on Si using a ZrO_2 gate dielectric. As a result of the high-quality ZrO_2/AlGaN interface and high dielectric constant of the ZrO_2, the AlGaN/GaN MOSHEMTs with a 30 nm gate dielectric exhibit a high on/off current ratio of 1.5×10^{10}, a steep subthreshold slope of 67 mV/dec, and a small hysteresis of ~0.1 V. The MOSHEMTs with a gate-drain distance of 20 µm show a high breakdown voltage of 980 V at a drain leakage current of 1 µA/mm.

INTRODUCTION

A high quality gate dielectric is one of the key elements to enable GaN-based metal-oxide-semiconductor high electron mobility transistors (MOSHEMTs) as reliable and energy-efficient power switches. MOSHEMTs with high-*k* gate dielectrics such as Al_2O_3 and HfO_2 have been investigated extensively [1-3], showing excellent device performance. Nevertheless, the dielectric constant of Al_2O_3 is still not high enough and the dielectric quality of HfO_2 on GaN needs further improvement. Alternatively, ZrO_2, which has a much higher dielectric constant than Al_2O_3, has attracted increasing research interest over recent years as the gate insulator for GaN MOSHEMTs [4-7].

Although ZrO_2 can be formed by various methods, ZrO_2 prepared by atomic layer deposition (ALD) shows the best dielectric quality. Nevertheless, the devices with a ZrO_2 gate dielectric in most of the previous reports still show relatively high leakage current and/or high density interface trap states, since the deposition conditions of ZrO_2 play an important role in the film properties and interface quality. To our knowledge, there are still limited results on GaN MOSHEMTs with the ZrO_2 gate dielectric showing low leakage and high breakdown performance.

In this paper, we present the device results of MOSHEMTs using ZrO_2 as the gate dielectric with superior gate stack quality. Low leakage current, high breakdown voltage, and minimal hysteresis have been obtained simultaneously.

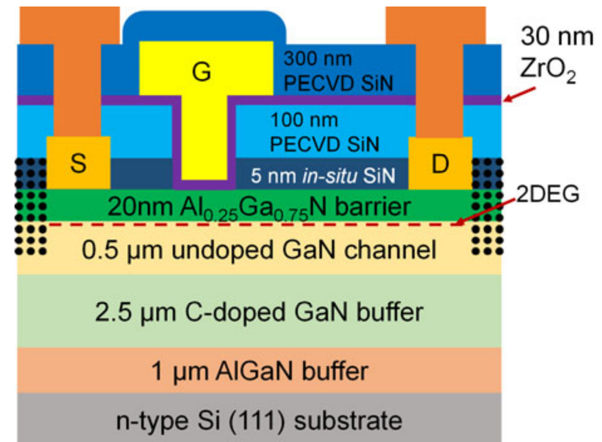

Fig. 1. Cross-sectional schematic of fabricated GaN MOSHEMTs.

DEVICE STRUCTURE AND FABRICATION PROCESS

Fig. 1 shows the cross-sectional schematic of the fabricated GaN MOSHEMTs. The employed epitaxial structure was grown on a 6-inch n-type Si (111) substrate by MOCVD, including a 1 µm step-graded AlGaN buffer, a 2.5 µm carbon-doped GaN buffer, a 0.5 µm undoped GaN channel, a 1 nm AlN spacer, a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 5 nm *in-situ* SiN cap. The device fabrication started with source/drain ohmic metallization, followed by a 100 nm plasma enhanced chemical vapor deposition (PECVD) SiN passivation. The device isolation was performed using argon implantation. The gate window was opened by removing both the PECVD SiN and *in-situ* SiN using a low power inductively coupled plasma (ICP) dry etching. After the barrier surface was cleaned by an HCl-based solution, a 30 nm ZrO_2 gate dielectric was deposited by ALD at 200°C. Then, the gate metal was formed by e-beam evaporation using a Ni/Au-based metal stack and the device was passivated with another 300 nm PECVD SiN. Finally, the Al-based pad metal was deposited. For comparison, a control sample with a Schottky-gate HEMT structure was also fabricated using the same as-grown wafer and the same process, except for the ZrO_2 deposition step. The devices discussed in this paper feature a gate foot length (L_G) of 2 µm, a gate head length of

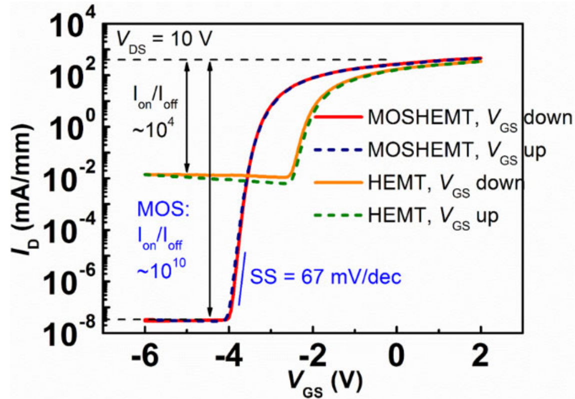

Fig. 2. Double sweep transfer characteristics of the MOSHEMTs and reference HEMTs at a V_{DS} of 10 V.

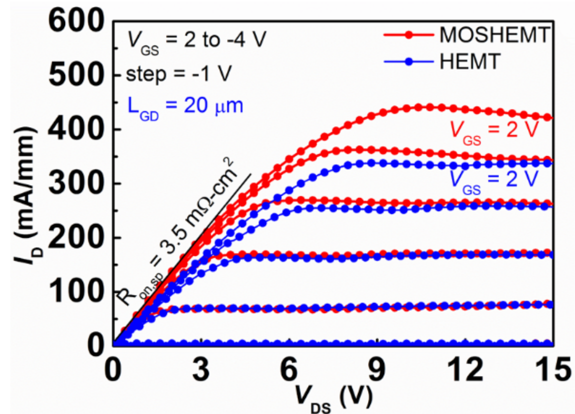

Fig. 3. Output characteristics of the MOSHEMTs and HEMTs.

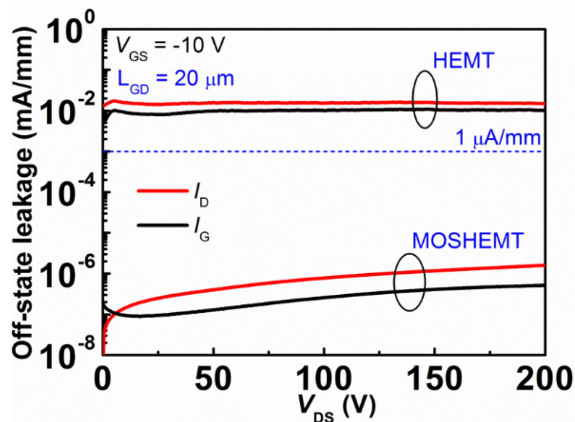

Fig. 4. Off-state drain and gate leakage current versus drain bias of the MOSHEMTs and HEMTs.

6 μm, a gate-source distance (L_{GS}) of 3 μm, a gate-drain distance (L_{GD}) of 20 μm, and a gate width (W_G) of 200 μm.

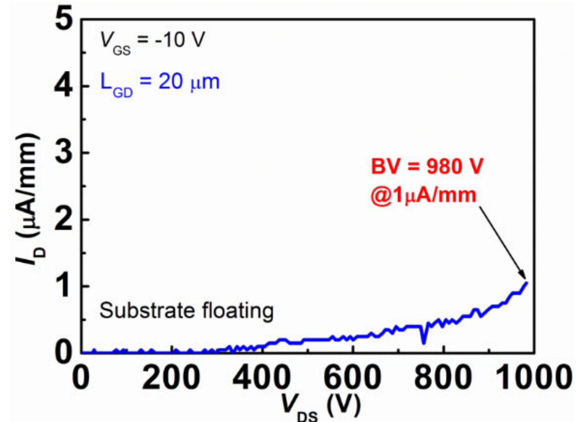

Fig. 5. Off-state I_D-V_{DS} of the MOSHEMT with a gate bias of -10 V.

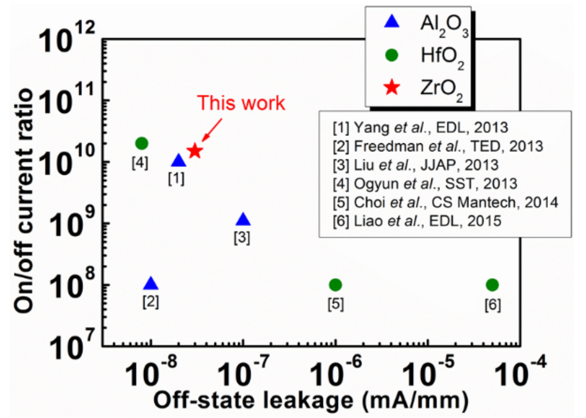

Fig. 6. Benchmarking of on/off current ratio versus off-state leakage current for MOSHEMTs with various high-*k* gate dielectrics.

DEVICE RESULTS AND DISCUSSION

Fig. 2 plots the double sweep transfer characteristics of a typical MOSHEMT and HEMT. The MOSHEMT exhibits an off-state I_D as low as 3×10^{-8} mA/mm, resulting in an on/off current ratio of 1.5×10^{10}, which is six orders higher than that of the HEMT. The MOSHEMT also shows a steep subthreshold slope of 67 mV/dec, as well as a negligible hysteresis of ~0.1 V, indicating a high-quality ZrO_2/AlGaN interface and efficient gate control over the channel. Moreover, the threshold voltage of the MOSHEMTs shift only -1.2 V with respect to that of the HEMT even though the gate dielectric is 30 nm thick, suggesting a strong capacitive coupling effect of the ZrO_2 and a low density of charges inside the ZrO_2 or at the ZrO_2/AlGaN interface. Fig. 3 compares the output characteristics of the MOSHEMTs and HEMTs. The I_{DS} of the MOSHEMT is 30% higher than that of the HEMT at a V_{GS} of 2 V. The specific on-resistance of the MOSHEMT is only 3.5 mΩ·cm^2. The off-state I_D and I_G as a function of drain bias V_{DS} are shown in Fig. 4. The I_D and I_G of the MOSHEMT are as low as ~1.6 nA/mm and ~0.5 nA/mm,

respectively, at a V_{DS} of 200 V and a V_{GS} of -10 V, four orders lower than those of the HEMT. The off-state breakdown voltage V_{DS} determined at an I_D of 1 μA/mm is as high as 980 V, indicating the effective leakage blocking capability of the MOS gate stack and good management of the peak electric field at the gate edge of the drain side. Fig. 6 benchmarks the on/off current ratio versus off-state drain leakage current of MOSHEMTs in this work with other state-of-the-art MOSHEMTs using high-k Al_2O_3 and HfO_2 gate dielectrics reported in the literature. The devices in this work exhibit an excellent on/off current ratio and low leakage current.

CONCLUSIONS

We have successfully demonstrated low leakage, high breakdown GaN MOSHEMTs on Si using a ZrO_2 gate dielectric. The devices showed minimal hysteresis, a steep subthreshold slope, and high leakage-blocking capability. The results suggest that ZrO_2 by ALD is a promising candidate as the gate dielectric in GaN MOSHEMTs for efficient power switching applications.

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REFERENCES

[1] J. J. Freedsman, T. Kubo, and T. Egawa, "High Drain Current Density E-Mode Al_2O_3/AlGaN/GaN MOS-HEMT on Si With Enhanced Power Device Figure-of-Merit 4 × 10^8 $V^2\Omega^{-1}cm^{-2}$," *Electron Devices, IEEE Transactions on,* vol. 60, pp. 3079-3083, 2013.

[2] X. Liu, C. Zhan, K. W. Chan, M. H. S. Owen, W. Liu, D. Z. Chi*, et al.*, "AlGaN/GaN Metal–Oxide–Semiconductor High-Electron-Mobility Transistors with a High Breakdown Voltage of 1400 V and a Complementary Metal–Oxide–Semiconductor Compatible Gold-Free Process," *Japanese Journal of Applied Physics,* vol. 52, p. 04CF06, 2013.

[3] C. Liao, X. Zou, C. W. Huang, J. Wang, K. Zhang, Y. Kong*, et al.*, "Low Interface Trap Densities and Enhanced Performance of AlGaN/GaN MOS High- Electron Mobility Transistors Using Thermal Oxidized Y_2O_3 Interlayer," *IEEE Electron Device Letters,* vol. 36, pp. 1284-1286, 2015.

[4] S. Rai, V. Adivarahan, N. Tipirneni, A. Koudymov, J. Yang, G. Simin*, et al.*, "Low Threshold-14 W/mm ZrO_2 /AlGaN/GaN Metal–Oxide–Semiconductor Heterostructure Field Effect Transistors," *Japanese Journal of Applied Physics,* vol. 45, p. 4985, 2006.

[5] G. Ye, H. Wang, S. Arulkumaran, G. I. Ng, R. Hofstetter, Y. Li*, et al.*, "Atomic layer deposition of ZrO_2 as gate dielectrics for AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors on silicon," *Applied Physics Letters,* vol. 103, p. 142109, 2013.

[6] R. Stoklas, D. Gregušová, K. Hušeková, J. Marek, and P. Kordoš, "Trapped charge effects in AlGaN/GaN metal-oxide-semiconductor structures with Al_2O_3 and ZrO_2 gate insulator," *Semiconductor Science and Technology,* vol. 29, p. 045003, 2014.

[7] T. J. Anderson, V. D. Wheeler, D. I. Shahin, M. J. Tadjer, A. D. Koehler, K. D. Hobart*, et al.*, "Enhancement mode AlGaN/GaN MOS high-electron-mobility transistors with ZrO_2 gate dielectric deposited by atomic layer deposition," *Applied Physics Express,* vol. 9, p. 071003, 2016.

ACRONYMS

MOSHEMTs: Metal-Oxide-Semiconductor High Electron Mobility Transistors
MOCVD: Metal-Organic Chemical Vapor Deposition
PECVD: Plasma-Enhanced Chemical Vapor Deposition
ICP: Inductively Coupled Plasma
ALD: Atomic Layer Deposition