Impact of Threshold Voltage Variation on RF Performance of 140 nm GaN MMICs

R. C. Fitch, Jr.[1], J. K. Gillespie[1], A. J. Green[2], D. E. Walker[1], Jr., D. Frey[3], J. Gassmann[3], M. Walker[3], G. H. Jessen[1]

[1]Sensors Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, Ohio 45433
robert.fitch.2@us.af.mil; 937-713-8883
[2]KBR Wyle Laboratories, Dayton, Ohio andrew.green.16.ctr@us.af.mil; 937-713-8842
[3]Cobham Advanced Electronic Solutions

Keywords: Gallium Nitride, High Electron Mobility Transistor, Monolithic Microwave Integrated Circuit

Abstract

X-Band power and low noise amplifier-based transmit/receive (T/R) monolithic microwave integrated circuits (MMIC) have been designed by Cobham into the Air Force Research Laboratory (AFRL) 140nm Gallium Nitride (GaN) dual-band process. Wafer-scale circuit, device and parametric parameters have been tracked across multiple process lots and epitaxy runs. Distributions of these parameters are compared with amplifier gain for hundreds of MMICs fabricated over multiple 4" SiC/GaN wafers.

Introduction

The Air Force Research Laboratory and Cobham Advanced Electronic Systems have collaborated on the development of an X-Band T/R MMIC fabricated in the AFRL GaN high electron mobility transistor (HEMT) 140nm baseline, dual-band process [1, 2]. Cobham's designs were employed on 18, 4-inch SiC/GaN wafers in two separate fab runs. The device models were generated by Modelithics from a prior fab run for specific device peripheries on devices designed by Cobham. These models were placed into the AFRL MMIC process design kit (PDK) that also provides standard passive components on a 100 um-thick SiC substrate. Circuit gain and frequency response closely matched the designs. Variation in HEMT threshold voltage was tracked against T/R gain and indicated a significant spread in performance for fab Run I. The root cause of this variation was related to a plasma ash tool which was unknowingly drifting out of specification and was an integral part of the critical e-beam lithography definition of the 140 nm gates. Upon instituting corrective actions, fab Run II proceeded and the threshold variation was reduced. Details of this process will be discussed.

Discussion

A scanning electron microscope (SEM) image of a portion of a fabricated MMIC is shown Figure 1. Included in the circuit are resistors, capacitors, inductors, micro strip lines, and an active HEMT. The HEMT devices are fabricated on

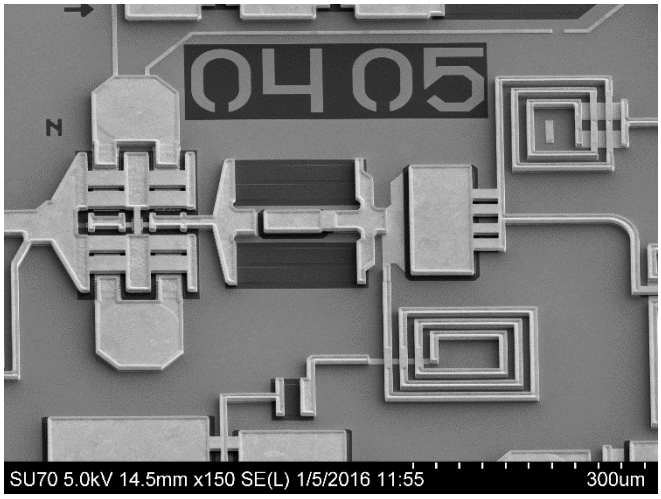

Fig. 1. Scanning electron microscope image of a portion a MMIC fabricated in the AFRL dual band 140 nm HEMT process.

IQE epitaxy with the following layers: GaN cap (30Å), $Al_{27}Ga_{73}N$ (158Å), Al (10Å), GaN (1.8um), AlN nucleation layer, SiC (500um). Figure 2 is a cartoon cross-section of the

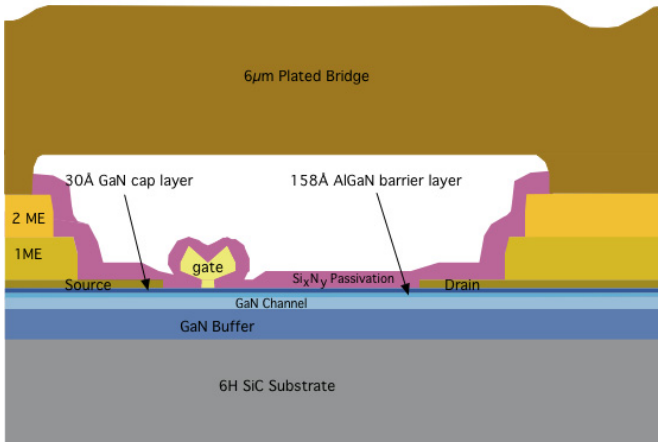

Fig. 2. Cartoon cross-section of the GaN HEMT.

HEMT on 6H SiC substrate. The front side process flow starts with the following: mesa definition by inductively coupled plasma chlorine-based etching down 700Å, and ohmic metal deposition by metal evaporation (Ti/200Å, Al/2000Å,

Ni/500Å, Au/500Å). The ohmic metal is used to define alignment key patterns for e-beam lithography of the T-gates. Ohmic metal on the devices is protected with photoresist during a chlorine etch of the alignment key patterns 1-um into the GaN buffer. Resistors are patterned in sputtered W_5Si_3 with a sheet resistance of 13 ohms/square. E-beam gates are deposited using a tri-layer stack of PMMA/MMA/PMMA with evaporated Ni/200Å, Au/3800Å. The last step prior to evaporation of the gate metal is a 30 second plasma ash to properly descum and size the gate stem. This step is extremely critical to ensure proper gate length and metal adhesion. Ti/200Å, Au/4800Å is deposited as interconnect metal and bottom plate for metal-insulator-metal (MIM) capacitors. 2000Å of silicon nitride device passivation is deposited at 300°C using plasma enhanced chemical vapor deposition (PECVD), then active device regions are protected with Micro-Chem LOR and 250°C silicon nitride is deposited with PECVD for capacitor dielectric. Capacitor breakdown exceeds 200V with a value of 300pF/mm^2. A nickel-based backside via-stop metal is then deposited on the pads where SiC vias will later be etched using plasma processing. A second interconnect metal of Ti/200Å, Au/4800Å is deposited prior to air bridge definition, which is the final front side process step. The post pattern, which defines the vertical separation between the bottom of the air bridge and the active transistor, is approximately 2.1 um of PMGI. A 1500Å gold seed layer is deposited onto the post pattern, and then the bridge pattern is defined using a negative resist AZ Electronic Materials 15nXT. The bridge metal is electroplated gold approximately 6 um's tall. The backside via processing was performed by GCS who thinned the wafer to 100 um's, etched backside vias, deposited backside gold ground plane metal and patterned saw streets.

Baseline dc electrical HEMT performance is illustrated in Figure 3, where the drain current density (J_d) and

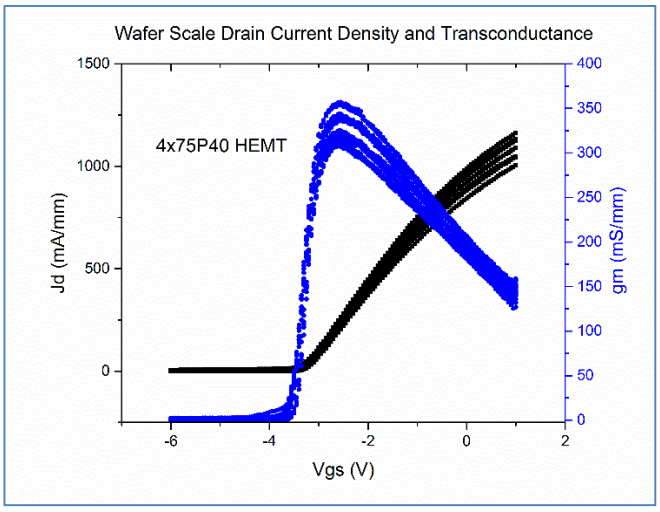

Fig. 3. Plot of drain current density and transconductance for nine dropout devices (4x75P40) across 4" SiC wafer RY141.

transconductance (g_m) are plotted for nine HEMT's measured from dropouts across 4" SiC wafer RY141. The HEMTs are 4-finger, 75um unit gate width devices with 40-um gate pitch (4x75P40). The nominal threshold voltage (V_{th}) for the modeled devices was targeted at -3.3 V, the extrinsic cutoff frequency (f_T) was 60 GHz, and the maximum oscillating frequency (f_{MAX}) was 103 GHz. Figure 4 shows the threshold voltage variation across 18 wafers where a clear demarcation is seen between Run I and Run II wafers. After Run I, the

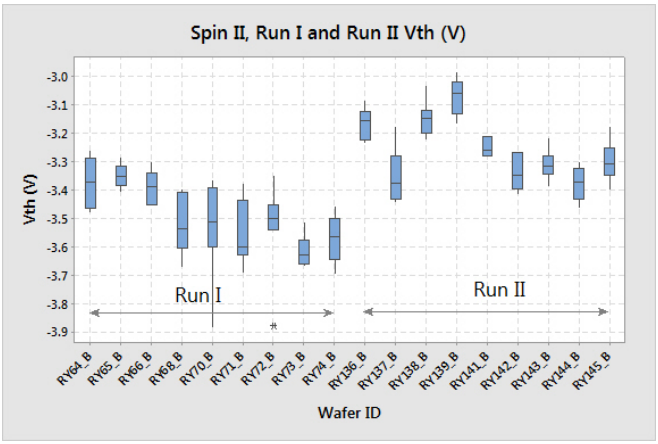

Fig. 4. Statistical distribution of Spin II, Run I and Run II threshold voltage for 18 wafers.

circuits exhibited a negative threshold shift from the design specification. Similarly, in Figure 5, a shift in extrinsic cutoff frequency is clearly seen. Higher g_m and f_T for the Run I wafers indicated probable shorter than nominal 140 nm gates

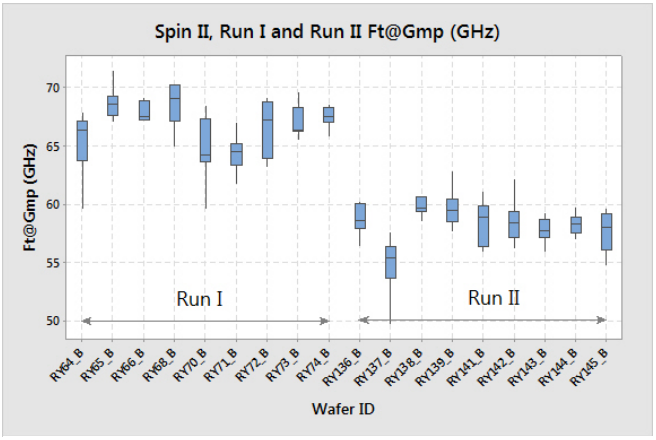

Fig. 5. Statistical distribution of Spin II, Run I and Run II extrinsic cutoff frequency for 18 wafers.

or a shift in the epitaxial AlGaN layer thickness or composition of Al. The nominal epitaxy AlGaN thicknesses were provided by IQE and specified on average 159 Å and [Al] = 27%. Therefore, gate length variation was the suspected cause for these variations.

ANALYSIS

In preparing for Run II processing, it was necessary to determine the root cause for the shift in threshold voltage from the design specification. Also, Run I had produced some wafers where the T-gates were not adequately adhering during subsequent process steps, and this issue provided a starting point for failure analysis.

A standard gauge is performed as part of the e-beam gate process module. Part of that gauge is to obtain the average gate length of at least five T-gate test structures across the wafer using an FEI DB235 dual beam focused ion beam (FIB) system. The typical T-gate cross-section of wafers in Run I is shown in Figure 6. The gate length is approximately

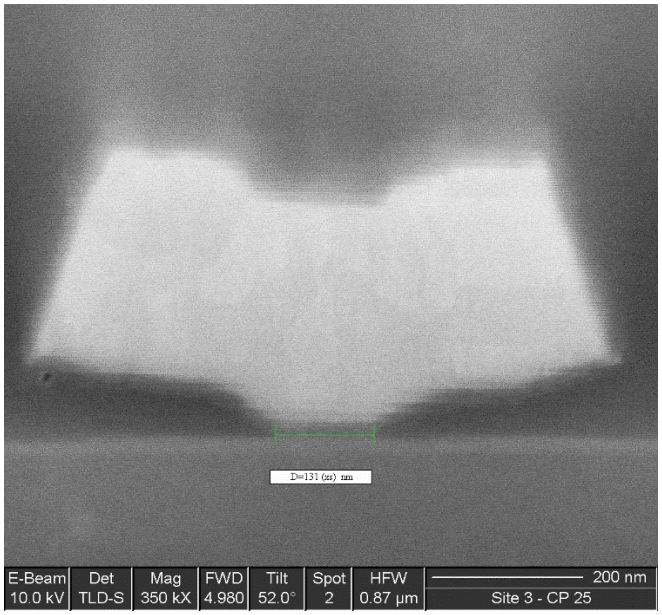

Fig. 6. Scanning electron microscopy image of the nominal T-gate cross-section for wafer RY66 from Spin II, Run I.

131nm, which is shorter than nominal. Also, the stem and wings appear non-standard as will be compared with the T-gate in Figure 7 which has the desired T-gate cross-sectional dimensions. This cross-section is from wafer RY143, and the gate profile exhibits a slight taper in the wings from the outermost tip of gold to the beginning of the stem, which slopes to the epitaxy surface at approximately 45°. The GaN/AlGaN top epitaxy layers are clearly seen in the image. The gate length is annotated at the Ni-GaN interface and measured 145nm.

From the dc electrical data and the facts that the gates were shorter than nominal and that they were not adhering adequately for the Run I wafers, a closer inspection of the e-beam T-gate process revealed that the LFE plasma asher was in question. Figure 8 illustrates the process pressure of the oxygen plasma at 20 seconds into the ash for 89 wafers. The suspect Run I wafers are boxed in red and were processed when a drop is process pressure was noted from the nominal 2.21 Torr. Examination of the asher revealed that the oxygen

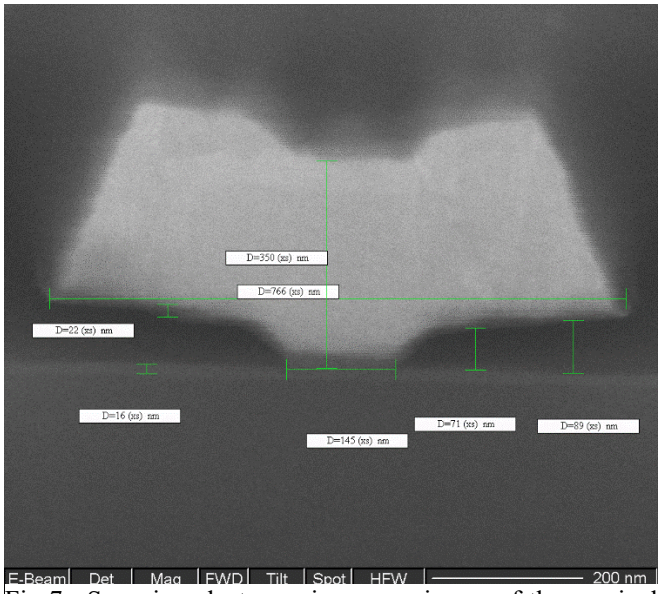

Fig 7. Scanning electron microscopy image of the nominal T-gate cross-section for wafer RY143 from Spin II, Run II.

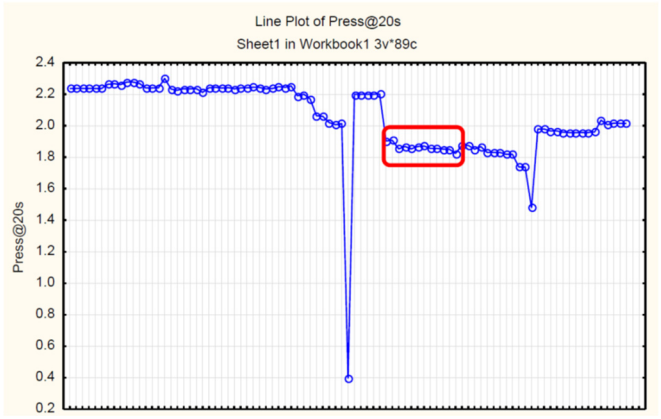

Fig. 8. Timeline of LFE asher pressure at 20 second point in the oxygen ash process.

mass flow controller was failing to deliver sufficient oxygen to the chamber causing an inadequate descum and shaping of the T-gate resist profile. A full design of experiments was performed on an Anatech plasma asher to re-center the ash process. The nominal gates fabricated in Run II are represented in Figure 7.

The threshold variations in the HEMT devices had a significant effect on the MMIC T/R performance as shown in Figures 9 and 10. These illustrate T/R gain plots with an insert of gate threshold voltage for all wafers from Run I. The darker data sets illustrate yielding circuits for the specified wafer. Optimal performance is achieved with the design threshold voltage of -3.3 V. Figures 11 and 12 illustrate the updated enhanced process capability characteristics for Spin II, Run II wafers for threshold voltage and extrinsic cutoff frequency of the standard 4x75P40 HEMT.

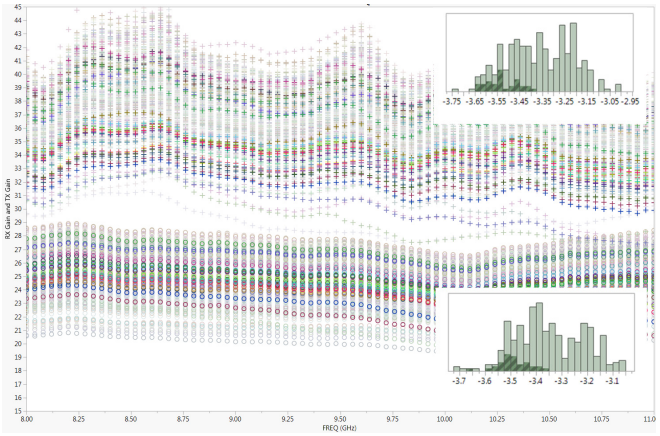

Fig. 9. Wafer RY74 TX and RX circuit gain with HEMT threshold voltage inserts (dark data sets); the more negative threshold voltage resulted in sub-par circuit gain.

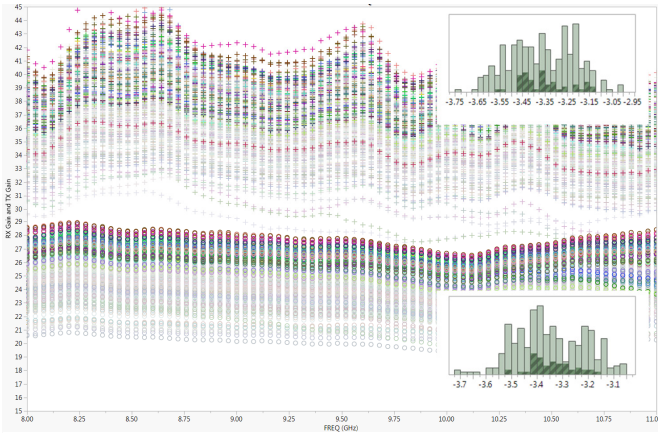

Fig. 10. Wafer RY68 TX and RX circuit gain with HEMT threshold voltage inserts (dark data sets) which matched the design value of -3.3 V (note tighter and higher gain results).

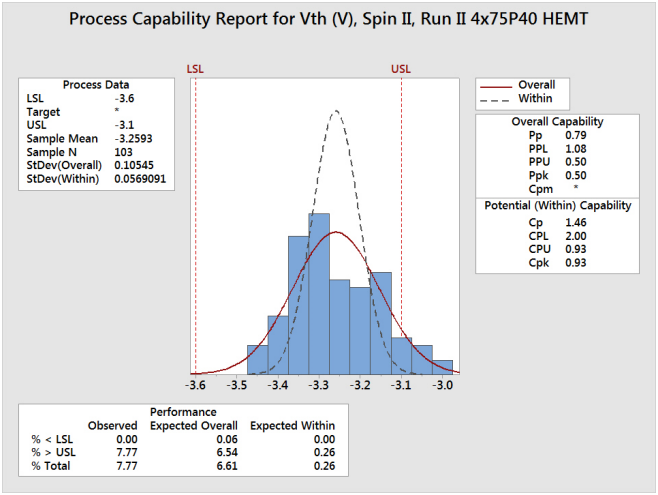

Fig. 11. Threshold distribution report for Spin II, Run II wafers and device 4x75P40.

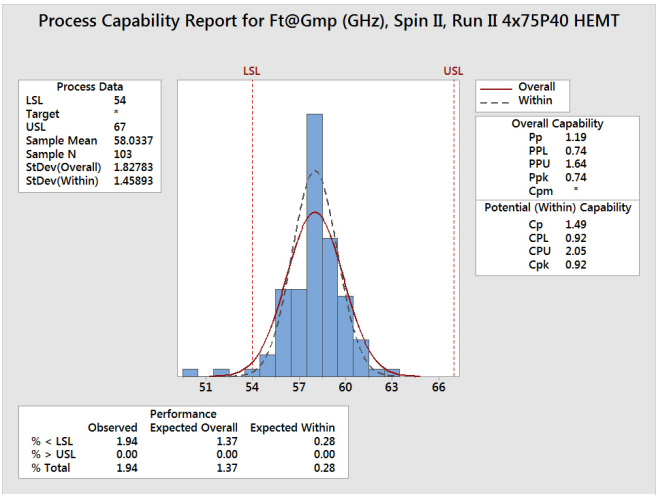

Fig. 12. Extrinsic cutoff frequency distribution report for Spin II, Run II wafers and device 4x75P40.

SUMMARY

The AFRL GaN 140nm HEMT MMIC dual band process was employed by the Cobham design team over two process runs of nine wafers each. The first run revealed a more negative device threshold voltage than the design value and was attributed to drift in a process tool. Corrective actions were implemented and the subsequent process run achieved threshold voltage values within 6-sigma of the design.

ACKNOWLEDGEMENTS

The authors would like to thank Mr. Andy Browning, Mr. Jason Hickey and Mr. Joe Breedlove for their cleanroom tool operation and maintenance to sustain the MMIC process.

REFERENCES

[1] R. C. Fitch, et al., Electron Device Letters, Vol. 36, NO. 10, October 2015.

[2] J. K. Gillespie, et al., *Demonstration of X-band T/R MMIC Using AFRL AlGaN/GaN MMIC Process*, 2016 CS MANTECH Technical digest, pp. 23--25, May 2016.

ACRONYMS

HEMT: High Electron Mobility Transistor
MMIC: Monolithic Microwave Integrated Circuit
FIB: Focused Ion Beam