Novel approach for E/D transistors integration in GaN HEMT technology

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Abstract

The purpose of this work is to introduce a novel concept for integrating enhancement mode (E-mode) and depletion mode (D-mode) AlGaN/GaN HEMTs in the same fabrication process. Unlike existing E/D integration technologies (gate recess etching, fluorine implantation etc.), the proposed technology does not involve process steps that damage the semiconductor layer and therefore more reliable devices are to be expected. The proposed technology allows control of 2DEG density under the gate region by means of external mechanical stress applied to the AlGaN barrier layer. The stress is introduced by a dedicated SiN_x passivation film. E and D – mode GaN HEMTs with state of art DC performance were fabricated on the same wafer using the proposed technology. Process flow for E/D transistors fabrication is presented as well.

INTRODUCTION

Despite the fact that nowadays GaN HEMT fabrication technology reached a readiness level that allows fabricating space and military qualified devices, there is a lack of truly normally-off and E/D integrated devices. Unlike GaAs technology, where normally-off transistors and E/D integration can be easily performed by chemical etching of the gate recess, in GaN technology such a solution is problematic due to the chemical inertness of GaN and its alloys and due to the significantly increased gate leakage current in recess etched enhancement mode devices. Therefore all attempts to achieve normally-off operation by plasma etching or fluorine implantation are still far away from production readiness level due to the not sufficient device reliability and performance that can be provided by these processes. The only true normally-off solution that is currently available on the market relies on GaN HEMTs with p-type doped gate structures [1]. However, this is a domain of GaN power electronics. In the presented work we offer an alternative solution that is based on the piezoelectric nature of the GaN material and allows a local decrease of 2DEG concentration underneath the Schottky gate. The effect produced by this technology is similar to the gate recess, but the process itself does not involve steps that can harm the semiconductor crystal and is therefore expected not to further deteriorate device performance and reliability. Another advantage of the proposed technology is the easy and inexpensive implementation in an existing GaN HEMT based process flow for MMIC fabrication. As the E- and D-mode transistors can be fabricated on the same wafer, the proposed technology facilitates fabrication of new types of circuits such as logic elements, ring oscillators etc. According to our belief this is one of the missing links in modern GaN HEMT technology.

PHYSICAL PHENOMENON AND SIMULATION RESULTS

The physical mechanism of the proposed local channel depletion effect bases on the piezoelectric properties of AlGaN and GaN. In an epi-grown AlGaN/GaN layer stack,

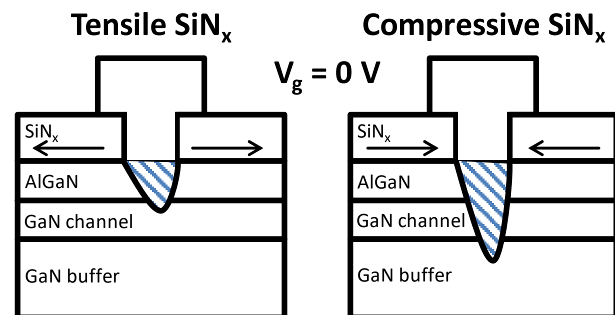

Fig. 1. Mechanism of GaN HEMT channel depletion by application of compressive external stress.

the AlGaN film undergoes tensile strain due to the lattice mismatch to the thick GaN buffer layer. This tensile strain leads to an increase of the piezoelectric component of polarization vector in the AlGaN layer and consequently

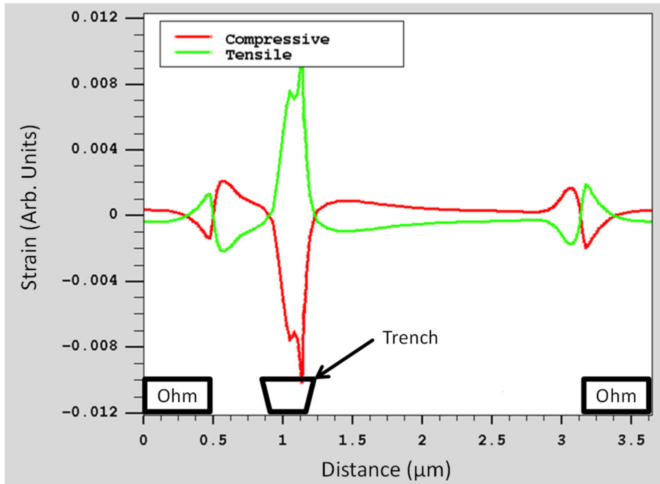

Fig. 2. 1D cut of simulated strain distribution in the middle of the AlGaN layer that is covered with compressively (red line) and tensile (green line) stressed SiN_x layers with etched trench.

increases the 2DEG concentration at the AlGaN/GaN interface [2]. The idea of the proposed technology is to locally decrease the piezoelectric component of the polarization vector under the gate by applying compressive external mechanical stress. In consequence the 2DEG density will decrease in the respective regions and, in conjunction with embedded the Schottky barrier, will lead to a partial or even complete depletion of the transistor channel (Fig. 1).

In order to theoretically confirm influence of the external mechanical stress on the 2DEG concentration under the gate trench Silvaco Athena in conjunction with Victory Stress module and Silvaco Atlas tools were used for simulation of AlGaN/GaN HEMT structures. After proper calibration, influence of internal SiN_x stress with magnitude ±1 GPa on the internal stress of AlGaN layer was investigated (Fig. 2). According to simulation the major change in mechanical strain occurs in the gate trench region and in those areas where the passivation is going over a metallic layer, in this case at the source and drain ohmic contacts. The drain access region is practically not affected. The effect is caused by a significant increase of the local internal stress of SiN_x film at the discontinuities in general (step or trench) as compared to the bulk material. Interestingly, a compressive SiN_x film creates a significant compression of the AlGaN barrier layer under the gate trench and a slight tension in the vicinity of the ohmic contacts. Both these effects are expected to be beneficial for GaN HEMT performance as local depletion under the gate (caused by AlGaN compression) leads to the possibility of normally-off operation, and local enrichment of 2DEG near the ohmic contacts (caused by tension of AlGaN) leads to decrease of contact resistance.

EXPERIMENT

Fabrication of E/D transistors started with growth of an AlGaN/GaN epitaxial structure on 4 inch n-type 4H-SiC

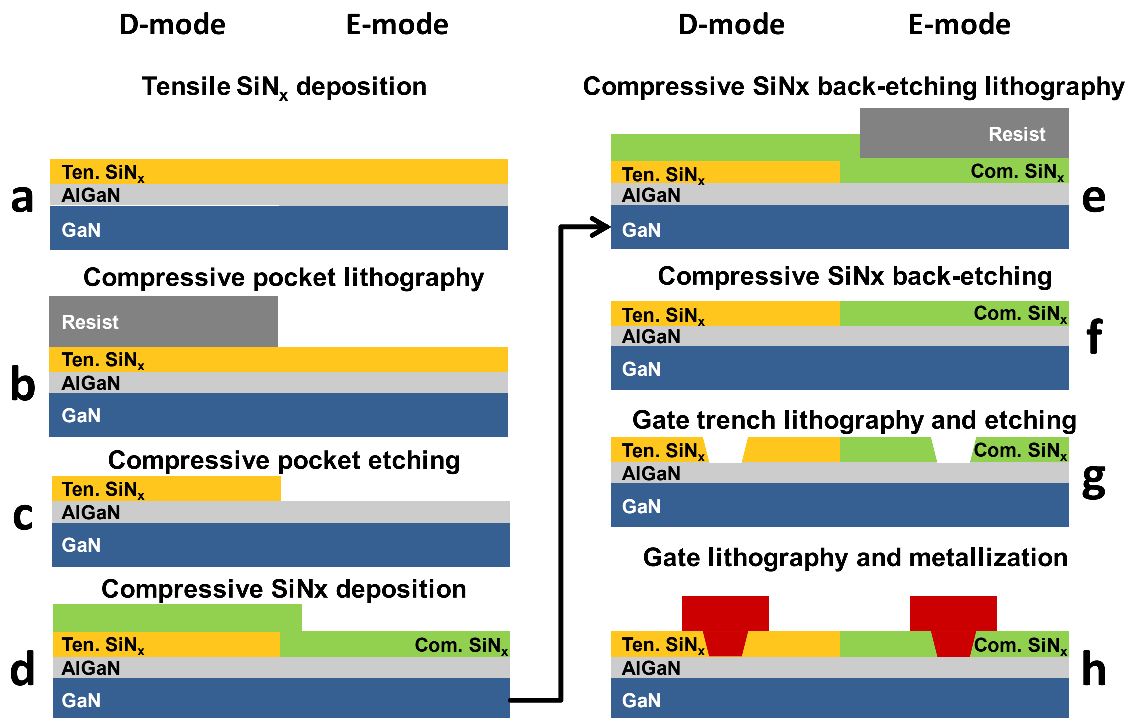

Fig. 3. Schematic representation of the process flow used for fabrication of integrated E/D transistors

substrate by low pressure MOVPE. An AlGaN barrier layer with a thickness of 10 nm and 26% Al concentration has been grown on top of an u.i.d GaN channel and a Fe doped GaN buffer layer resulting in an average sheet resistance of about 550 Ohm/□. A Ti/Al based metal stack was used for the formation of ohmic contacts with an average contact resistance of 0.5 Ohm/mm. After ohmic contact fabrication a 300 nm thick tensile SiN_x passivation layer was first deposited on the whole wafer (Fig. 3 a). Afterwards window openings in this passivation layer were realized by photolithography and dry etching at locations where the normally-off (E-mode) transistors have to be placed later (Fig. 3 c). A compressive SiN_x passivation layer was then deposited on the whole wafer and subsequently removed from the locations of the normally-on (D-mode) transistors again, by using photolithography and dry etching steps (Fig. 3 g). After that FBH´s genuine "Sputtered Ir" process flow as described in [3] was used in order to finalize fabrication of 100 nm gates (Fig. 3 h).

TABLE I
DC PERFORMANCE OF E- AND D-MODE TRANSISTORS

Property	D-mode	E-mode
I_{ds_max} (A/mm)	1.1	0.67
V_{th} (V)	-1.1	0.3
g_{m_max} (mS/mm)	440	430
I_{gs_leak} (A/mm)	1×10^{-4}	5×10^{-8}

DC PERFORMANCE

After transistor fabrication DC characterization was performed. Table 1 shows the DC performance of the obtained transistors. As can be seen, the threshold voltage difference between E- and D-mode transistors is more than 1 V. At the same time the DC performance of E-mode transistor exceeds the state of art values known to us for AlGaN/GaN HEMTs in terms of R_{on}, peak transconductance and gate leakage current. This performance is due to the fact that the new technology practically provides a "virtual" gate recess effect while maintaining the thickness of the AlGaN barrier layer constant. Another factor defining good performance is nearly ideal Schottky barrier quality provided by the "Sputtered Ir" gate technology and absence semiconductor surface damage introduced by fabrication process. This first of all allows a nearly ideal normally-off behavior; additionally, the transistor access region resistances are not compromised by specific normally-off technology trade-off between AlGaN thickness and V_{th} resulting in low parasitic input and output resistances.

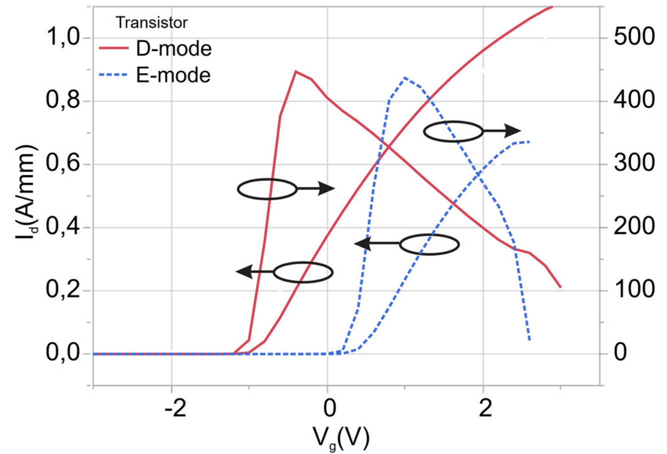

Fig. 4. Transfer characteristics and transconductance of monolithically integrated E- and D-mode transistors.

At the same time DC performance of D-mode transistors corresponds to the existing state of art. Fig. 4 shows transconductance and G_m curves for E- and D-mode transistors. As can be seen, maximum drain current obtained for E-mode transistors is more than half of current of D-

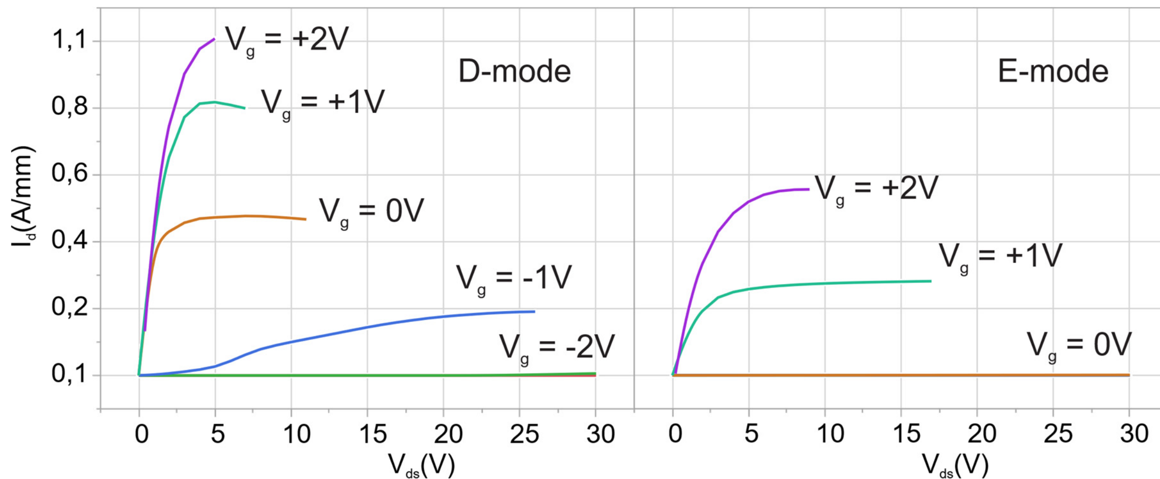

Fig. 5. Measured DC output characteristics for E-mode transistors (right) and D-mode transistors (left).

mode devices. Additional measurements of the source resistance and R_{sh} revealed big differences between D-mode and E-mode devices. Measured source resistances were about 0.6 Ohm*mm and 0.9 Ohm*mm for D- and E-mode devices respectively. The reason of this difference is epi sheet resistance that was about 410 Ohm/□ for normally-on and 1100 Ohm/□ for normally-off transistors. The reason of this discrepancy is a potential damage of the semiconductor surface during backetching of the tensile SiN_x layer in the area of the normally-off devices (Fig. 3 c). Extracting the intrinsic transconductance by de-embedding the data with the measured source resistance values resulted in 600 mS/mm for D-mode and 700 mS/mm for normally-off transistors. As the barrier thickness is the same for both kinds of transistors one can speculate that increase in the maximum transconductance observed for the normally-off devices is caused by increase of electron saturation velocity due to decrease of carrier-carrier scattering in the more depleted channel of the normally-off device.

Fig. 5 shows the output characteristics of the obtained transistors. The E-mode device clearly shows a lower maximum current than the D-mode device. As mentioned above this is in part due to potential etch damage during back-etching of the tensile nitride. Nevertheless, despite of this processing issue the maximum drain current of the E-mode transistors is competitive to other normally-off device technologies. The D-mode devices have a rather high drain current, but they are suffering from punch-through effect (branch at V_g = -1 V). In contrast the E-mode devices have a good pinch-off performance and remain closed at V_g = 0 V till V_{ds} = 30 V. These results confirm the recess-like effect of the proposed technique and an efficient suppression of short-channel effects for short gate devices.

Fig. 6 demonstrates that the local tensile strain caused by the compressive SiN_x layer at the step between ohmic contact and the AlGaN barrier layer surface (see also Fig. 2) has quite a beneficial effect: It clearly reduces the ohmic contact resistance. The additional tensile strain at the ohmic contact edge locally increases electron concentration and in consequence assists electron injection from the ohmic metal to the channel. According to Fig. 6 TLM structures coated with compressive SiN_x layer clearly demonstrate this effect. They show an average contact resistance about 0.25 Ohm*mm as compared to 0.36 Ohm*mm for the same structures covered with the tensile nitride layer – a reduction of the ohmic contact resistance by typically 30%.

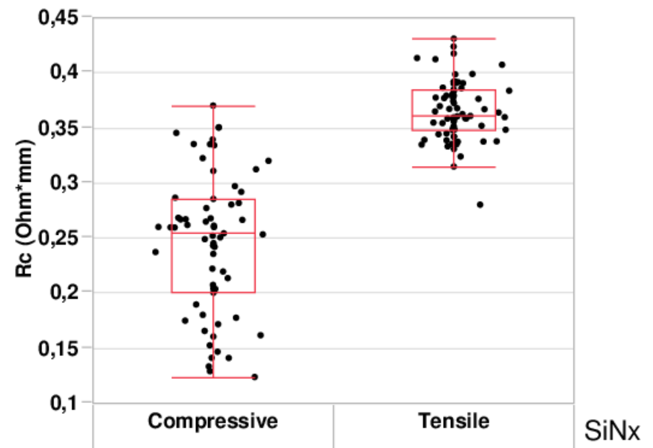

Fig. 6. Ohmic contact resistance measured on TLM structures covered with compressive and tensile SiN_x layers.

Conclusions

A novel approach for the integration of E/D transistors in AlGaN/GaN HEMT technology was demonstrated. It has been proven experimentally, that use of a dedicated SiN_x passivation layer as an external mechanical stressor allows significant change of the piezoelectric component of polarization vector in AlGaN barrier. Compressive SiN_x locally depletes the 2DEG under the Schottky gate and enriches the 2DEG in the vicinity of the ohmic metal step. E- and D-mode transistors were fabricated using the proposed approach by adding 5 additional process steps to the conventional Ka-band GaN MMIC process established at FBH. DC electrical performance of the obtained E- and D-transistors shows that it is possible to realize normally-off transistor by applying localized compressive strain underneath the gate. This technique has been combined with excellent nearly dispersion free Schottky barrier quality due to the “Sputtered Ir” approach. The proposed process flow modification is quite scalable and can be generally used for obtaining transistors with different separately engineered threshold voltages on the same wafer. This potentially facilitates the monolithic integration of different circuit types such as PA, LNA, driver and many more.

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