An Improved 0.25µm GaN on SiC MMIC Technology for Radar and 5G Applications

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Keywords: AlGaN/GaN, High electron mobility transistor, 0.25µm, GaN on SiC, 5G

Abstract

An improved 0.25µm GaN HEMT technology has been created by optimizing the fabrication process and the epitaxial layer structure. The pulsed I-V characteristics have been improved with typical gate-lag and drain-lag of 16% and 6%, respectively. The transistor for RF power amplifier use has the small signal gain improved by 1.8dB up to 20.3dB, the power density 3dB into compression increased from 4.2 to 4.7W/mm, and the maximum power-added efficiency improved from 59.6% to 64.7% at 10GHz. The transistor for RF switch use exhibits switching speed of 13.1ns on falling edge and 35.8ns on the rising edge of output signal. The changes to the process have resulted in enhanced HTRB reliability performance with a signature of leakage current being significantly suppressed over time providing stable and reliable operation.

INTRODUCTION

The applications for which GaN on SiC power cells and MMICs have expanded to not only include X-band AESA phased-array radar driven by defense application but also various commercial applications including Ku-band VSAT, broadband amplifiers from 6-18GHz, and massive MIMO base station applications below 6GHz for 5G needs. The start of the setting of specification for 5G occurred earlier this year with release 14 of the 3GPP New Radio 5G specs.

The 0.25µm MMIC-capable GaN on SiC technology (NP25) is well suited to address the needs of these markets and further improvements to this technology have been realized and will be presented here. Large-signal power performance in regard to gain, output power density and power-added efficiency are improved by re-engineering the epitaxy and optimizing process conditions. An RF switch with good switch speed that is complementary to the power amplifier is added to this process technology and will be discussed further.

TECHNOLOGY REVIEW

The AlGaN/GaN HEMTs and MMICs are fabricated on 100mm GaN-on-SiC wafers using a dedicated 100-mm wafer manufacturing line. The Ti/Al based Ohmic contacts are formed on top of semiconductor surface and followed by a PECVD-deposited, 1st Silicon Nitride (1st SiN) passivation layer. Device isolation is realized by using multiple energy boron ion implantation. A low-damage gate dielectric etch is performed to define the foot of the damascene gate and then re-aligned Ni/Au-based T-gates are deposited creating a gate-coupled field-plate structure. A 2nd SiN layer is then deposited over top of the gate followed by a source-coupled field-plate (SFP) whose function is to suppress the electric field near the edge of the gate at the semiconductor surface, deplete surface states and to reduce gate-to-drain feedback capacitance (C_{GD}) enabling small- and large-signal gain enhancement. Subsequently the passive components and interconnect stack are formed and begin with thin-film TaN resistors with sheet resistivity of 50Ohm/square, interconnect metal layers named MET0, MET1 and MET2 with 0.6, 1.1 and 4.0µm thickness, respectively, and formed of Au-based metal. A high breakdown voltage metal-insulator-metal (MIM) capacitor is formed by MET1/3rd SiN/MET2 to withstand breakdown voltage exceeding 200V and with a mean-time-to-failure (MTTF) of 20years when operated in DC, stressed at 60V at an ambient temperature of 125°C. After front-side processing, the SiC substrate is thinned down to 100µm, followed by back-side through via etching. The vias are 30 x 60µm oval vias lined with Ti-based seed layers and a total of 5.5µm of Au metallization. A SEM cross-section of a GaN device is shown in Figure 1.

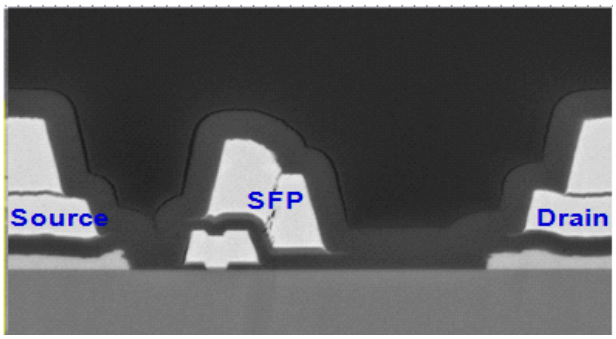

Fig. 1. An SEM cross-section of the AlGaN/GaN HEMT designed for power amplifiers in the improved 0.25µm GaN on SiC process

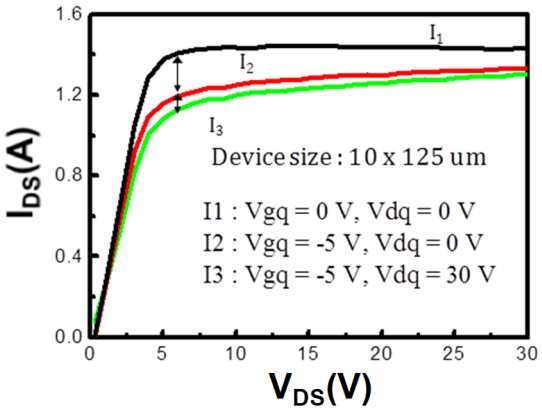

Fig. 2. Pulsed I_{DS}-V_{DS} output characteristics of the revised NP25. I_1, I_2, and I_3 are the drain currents with different quiescent biases. Gate- and drain-lag are defined by (I_1-I_2/I_1) and $(I_2-I_3)/I_2$, respectively.

Since nonlinear behavior, frequency dispersion, and thermal characteristics of power devices dominate RF performance such as PAE, the accuracy of the large-signal model is critical to design power amplifiers, especially for GaN MMICs. A process design kit (PDK) includes a large-signal scalable HEMT model. The model accounts for dispersion effects (gate-lag and drain-lag phenomena), due to carrier trapping, extracted from pulsed IV and transient characteristics, and is modeled using trap sub-circuits. A thermal RC sub-circuit is also included in the equivalent circuit model to simulate the self-heating effect. The model also provides an external thermal node to which customers can connect their own sub-circuits based on the thermal management at the package level.

Device Characteristics Comparison in Previous and Revised Process

In general, AlGaN/GaN HEMT devices suffer from current collapse in pulsed IV measurements and kink effects in DC output characteristics, all of which lead to degradation of RF performances. These mechanisms are mainly due to trapping/de-trapping effects [1]. Gate-lag and drain-lag are common methods to monitor the trapping effects near the semiconductor surface and in the epitaxy buffer layer, respectively.

Figure 2 shows the pulsed IV characteristics in the revised NP25. Pulsed IV measurements are carried out with pulse duration of 750ns and the pulse conditions are sufficiently fast to remove self-heating effects. The three curves of I_1, I_2, and I_3 corresponds to pulsing from three different quiescent points of (V_{GS}=0V, V_{DS}=0V), (V_{GS}=-5V, V_{DS}=0V) and (V_{GS}=-5V, V_{DS}=30V) to bias conditions in the I_{DS}-V_{DS} plane. The gate-lag and drain-lag ratio are defined as $(I_1-I_2)/I_1$, $(I_2-I_3)/I_2$, respectively, at V_{GS}=1V and V_{DS}=6V. The previous NP25 device shows gate-lag and drain-lag of 23.3% and 11.6%, respectively. The revised NP25 shows significantly suppressed gate-lag and drain-lag ratio of 15% and 5.1%, respectively. The gate- and drain-lag are mainly reduced by changes in the gate module including gate metal stack, surface pretreatment prior to gate metallization and by changes to the epitaxial layer structure and growth.

DC output characteristics of transistors in the previous and revised NP25 are shown in Figure 3. The V_{GS} is swept from -3 to 0V in steps of 0.5V and the V_{DS} is varied from 0 up to 60V. The device in the previous NP25 shows clear kink effects which are absent in the revised NP25. The kink effect originates from trapping, at low V_{DS}, and de-trapping, at high V_{DS}, of hot electrons. This results in the threshold voltage shifting toward more negative voltages and a consequential, sudden increase of I_{DS} in the DC output characteristics [2]. The kink becomes more severe as the maximum drain voltage is swept to higher bias voltage. These deep traps are located within the epitaxial layers underneath the gate.

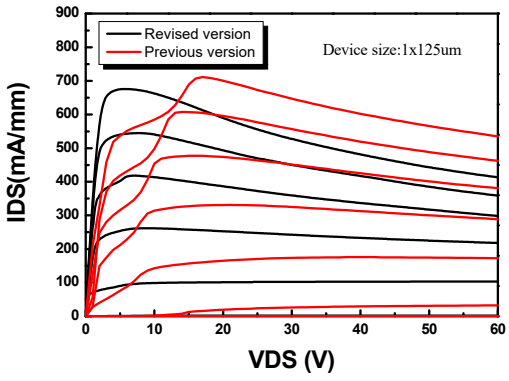

Fig. 3. DC output characteristics comparing previous and revised NP25. V_{GS} is swept from -3 to 0V with steps of 0.5V and V_{DS} is swept up to 60V.

Figures 4(a) and (b) show comparisons of the small signal and load-pull performances of AlGaN/GaN HEMTs in the previous and revised NP25 processes, respectively. The

devices were biased at an operating voltage of 28V and a quiescent drain current of 100mA/mm for both small-signal and load-pull characteristics, where the device size of 2x125µm and the test condition are identical for comparison.

As shown in Figure 4(a), the unity current gain cut-off frequency (f_T) exhibits no difference in the previous and revised NP25. The revised NP25 shows a power gain of 20.3dB at 10GHz, which is ~1.8dB higher than that of previous NP25 with a power gain of 18.5dB. Through small signal analysis, the improved small signal gain in the revised NP25 is mainly attributed to a decrease of the output conductance g_{DS}. The feedback capacitance of C_{GD} and the drain-to-source capacitance of C_{DS} both show similar values in the two different technologies. This indicates that the increased C_{GS} and gm are compensated and result in almost the same f_T. The increase of C_{GS} can be mainly attributed to

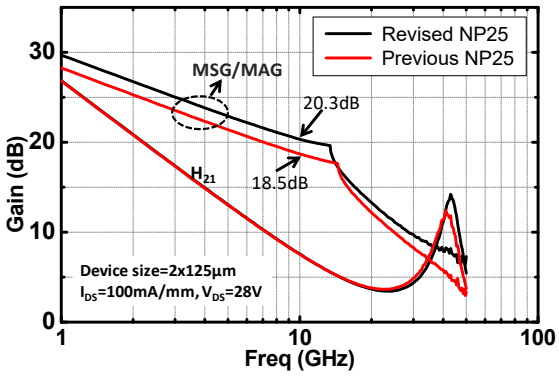

Fig. 4 (a)

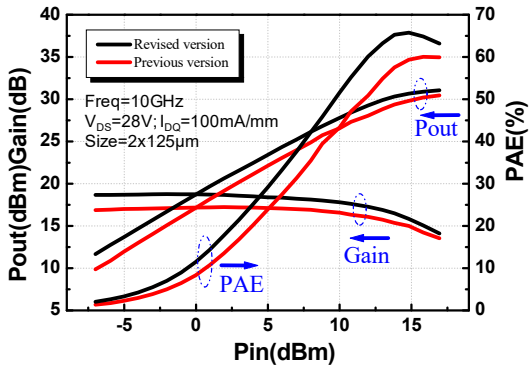

Fig. 4 (b)

Fig. 4 On-wafer (a) small-signal and (b) load-pull performance comparisons in the previous and revised NP25. The devices are tuned for maximum efficiency and operated in continuous-wave (CW) mode for the load-pull measurements.

the 1st SiN passivation. A Silicon-rich PECVD SiN film is introduced into the revised NP25, which reduces surface trap states near the un-gated access regions of the transistor. This film also has an increased dielectric constant.

As shown in Figure 4 (b), the on-wafer load-pull characterization at 10GHz was performed in continuous-wave (CW) mode with only the fundamental tuned at the source and load. A maximum PAE of 59.6 and 64.7%, and a linear gain of 16.9 and 19.0dB were obtained for devices from the previous and revised NP25 process, respectively. The devices from the revised NP25 process show improved output power density at the 3dB compression point of 4.7W/mm, which is 12% higher than that of 4.2W/mm in previous NP25 process.

DC-HTOL and HTRB high-temperature reliability test have been performed and passed qualification in the revised NP25. A 2x125µm device was chosen as a test vehicle in the reliability test. The key parameter of normalized saturation drain current (I_{DSS}) is monitored continuously over time in the DC-HTOL and HTRB test, as shown in Figures 5 and 6, respectively. In addition to I_{DSS}, off-state 3-terminal drain leakage current (I_{PO}) are included in our reliability qualification tests. Each parameter was measured at room temperature for different instances in time during the full period of the test. The DC-HTOL was performed at a bias voltage of 28V, a drain current of 300mA/mm, and a junction temperature of ~250°C. The junction temperature was

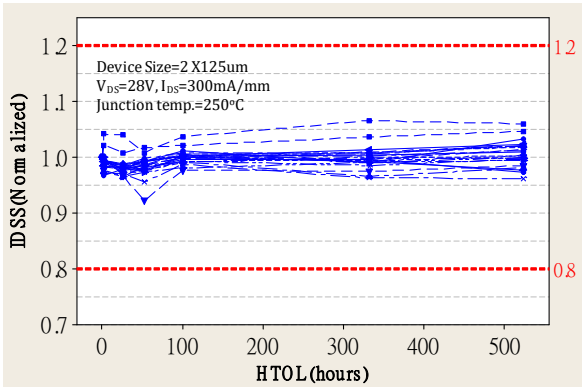

Fig. 5. The normalized I_{DSS} (I_{DS}@V_{GS}=0V) during DC high-temperature operating life time (DC-HTOL) test.

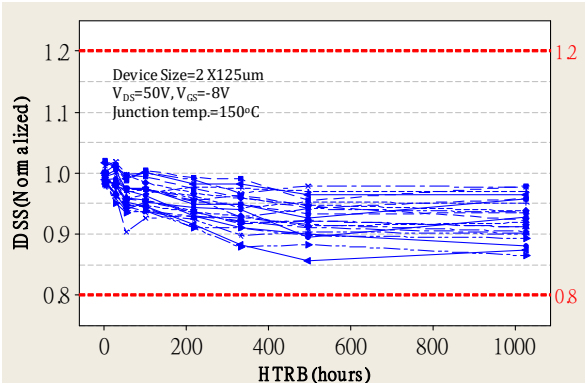

Fig. 6. The normalized I_{DSS} (I_{DS}@V_{GS}=0V) during DC high-temperature operating life time (DC-HTOL) test.

through using Micro-Raman measurements. The drain leakage current was measured at V_{DS} of 28V and V_{GS} of -8V,

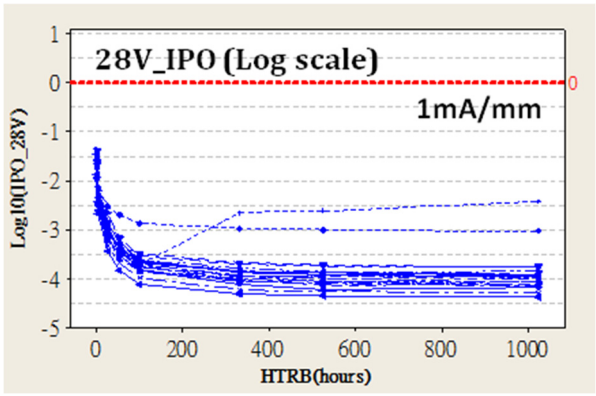

Fig. 7. Normalized off-state 3-terminal drain leakage current (28V_I_{PO}) at V_{GS}=-8V and V_{DS}=28V during high temperature reverse bias (HTRB) test.

shown on a logarithmic scale in Figure 7. The leakage current decreased over time and saturated after 100hrs at current level around 1 to 10µA/mm. The drain leakage current was measured at V_{DS} of 28V and V_{GS} of -8V, shown on a logarithmic scale in Figure 7. The leakage current decreased over time and saturated after 100hrs at current level around 1 to 10µA/mm. The HTRB test was performed at a V_{DS} of 50V and V_{GS} of -8V and ambient temperature of 150°C.

RF Switching Characteristics in The Revised NP25

Recently, an RF switch development has been completed in the revised NP25 process and the performance has been characterized including the critical parameters of switching time, on-resistance (R_{ON}) and off-state capacitance (C_{OFF}). This new development provides an opportunity to have a technology platform with full integration of RF switch and RF power amplifier design simultaneously.

The RF switch device is a symmetric transistor with a 0.25µm gate located at the center of source-drain region and is without a source-coupled field-plate. A standard RF switch test device is 9x100µm in size in common-gate configuration connected with a gate series resistor of 40kΩ by using a mesa resistor. The test setup configuration is shown in Figure 8. An RF signal at a frequency of 1GHz and a power level of 25dBm is excited at the input to the RF switch and an envelope detector is connected at the output port. The output current waveform is observed by using an oscilloscope. A pulse generator at the gate was used to drive the device from on-to-off and off-to-on states. The test used a pulse width of 50µs with a duty cycle of 10%.

The rise time and fall time of the switching characteristics are defined to be the time required for current response to go from 10% or 90% of the pulse step height from off-to-on and from 90% to 10% for on-to-off, respectively. The gate is pulsed from 0V to -22V and from -22V to 0V, respectively. The RF switch device in the revised NP25 technology exhibits a rise time of 35.8ns and a fall time of 13.1ns. An R_{ON} of 3.1Ω-mm and C_{OFF} of 186.7fF/mm are extracted at 100MHz.

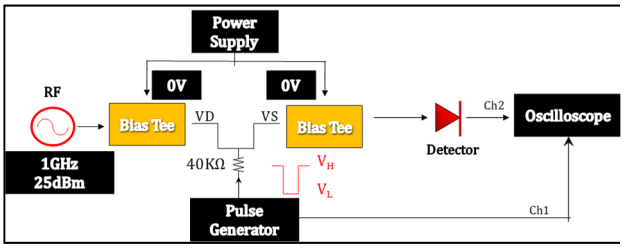

Fig.8 RF switch test system configuration.

HTRB has been performed for an RF switch device in the revised NP25. The HTRB test is done at a gate bias of -50V with the drain and source grounded and at an ambient temperature of 150°C. A 2x125µm device is chosen as a test vehicle. The key parameter of normalized on-resistance R_{ON} is monitored over time as shown in Figures 9. The threshold voltage, saturation drain current are also monitored in our reliability qualification tests but are not shown here. All parameter variations for the HTRB test are within 12% demonstrating that reliable operation of an RF switch is realized in the revised NP25 platform.

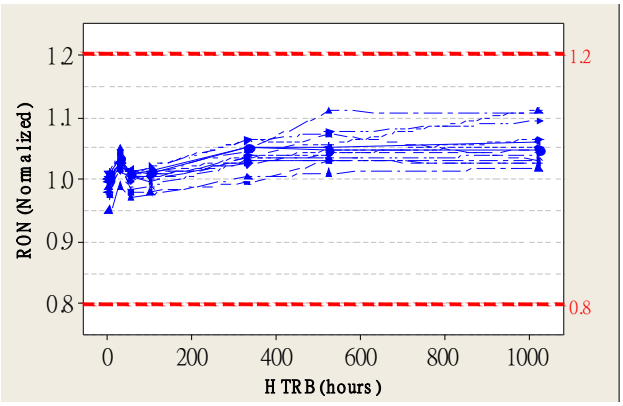

Fig. 9 Normalized on-resistance (R_{ON}) during high-temperature reverse bias (HTRB) test.

Conclusion

Significant improvements to the NP25, 0.25µm GaN on SiC MMIC technology have been presented. RF large-signal performance for the power amplifier transistor has a small signal gain of 20.3dB, power density of 4.7W/mm, and maximum power-added efficiency of 64.7% at 10GHz. Switching speed for the RF switch is below 50ns with R_{ON}-C_{OFF} product of 0.6psec.

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