Mechanism and Resolution of Implant Induced ESD Damage in GaAs IC Processing

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Abstract

In GaAs fabrication, electro static discharge (ESD) failure is a major liability concern impacting both yield and device reliability. This paper describes a set of circumstances at the isolation implant step involving the design layout, process sequence and tool configuration that formed the ideal condition for a surge of electrostatic related defects. After a series of experiments, the primary source and mechanism of the failure were identified, leading to key process improvement measures that ultimately enhanced the device robustness against ESD damage.

INTRODUCTION

He++/He+ ion implantation is a common method used in GaAs processing to achieve device isolation. Due to the inherent nature of ion implantation, charge build-up takes place on the wafer. Elimination of the damaging effects of electrostatic discharge on the devices on the wafer is a challenge, especially if there are sufficient numbers of metal contacts present on the wafer prior to the ion implant process. This paper explores the yield impact, mechanism and potential solutions to the ESD failures in GaAs HBT fabrication caused by ion implantation.

Typically, the isolation implant process is introduced early in the GaAs processing flow with no or very low density of metal contacts on the surface of the GaAs wafers. This is to avoid any potential yield impact caused by ESD damage as a result of the build-up of charge on the metal and wafer surface during the implant step. In circumstances where metal contacts are necessary prior to implant, the size and area of each contact must be minimized to prevent excessive ESD failures. A severe example of this occurred during a new HBT technology node development where the combination of ohmic metal contacts in an HBT array passivated by protective SiNx (nitride) layer and coated with photo resist prior to implantation created the critical environment for the tremendous damage caused by electrostatic discharge. These ESD defects shown in Figure 1 contributed to both visual and probe failures and accounted for about 0.5% yield loss. The visual failure was captured by the inline optical (August tool) inspection and the probe yield loss was caught at the functional leakage test.

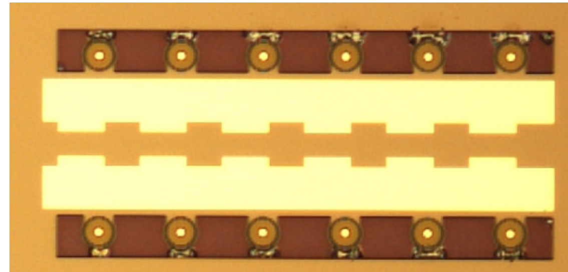


Figure 1. ESD defects on HBT transistor array

FAILURE MECHANISM

In an effort to identify the source of the electrostatic discharge, a sequence of experiments was conducted which included different types of epitaxial materials, photo resists, nitride film densities and implanters at various facilities. All of these factors provided no improvement to the ESD failure. On the other hand, some of the evaluations did produce strong correlations between the extent of electrostatic damage and several essential process and tooling parameters thus providing valuable insights into the mechanism of this failure.

Wafers passivated with unpatterned photo resist and nitride films were observed to have the most severe ESD defects. Wafers that were cycled through the implanter without receiving any implant processing did not exhibit any ESD damage which implied the charging of wafers occurred during the implant process. Furthermore, reducing the implant beam current seemed to have a direct impact to the severity of the ESD damage and the failures appeared to be area dependent impacting the larger metal features considerably more than the smaller, isolated ones. Interestingly, in extreme cases, the ESD damaged structures on the wafer followed a cross pattern as displayed in Figure 2. This pattern was later identified to mirror the grounding path of the electrostatic chuck (ESC) on the EATON/Axcelis 8250 ion implanter system. All of the above findings were critical in explaining how the implanted charges were distributed across the wafer, how excess charges built up at certain locations on the wafer and how these charges dissipated through the ESC chuck to ultimately generate these devastating failures.

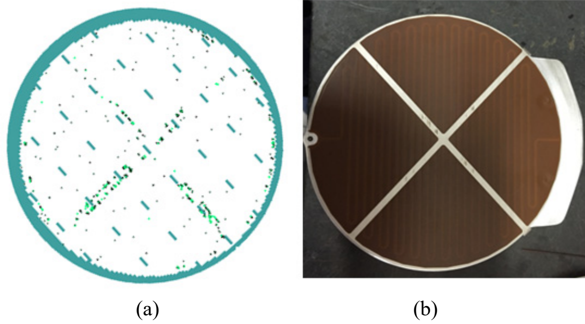

(a) (b)

Figure 2(a) Yield map with cross-hair ESD failures (b) the Implanter ESC chuck ground path in a cross and ring pattern with the grounding pin to the left of the chuck.

The EATON/Axcelis 8250 implanter ESC chuck is uniquely designed for GaAs processing with the chuck divided into four equal quadrants so that the polarity of these sections can be reversed to allow for better release of the wafer after the implant process. The four sections of this ESC are laid out in a cross configuration within the outer edge ring as seen in Figure 2(b). The entire surface of the ESC is coated with an insulating polymer except for the cross-hair and outer ring areas which are used to ground the substrate through grounding pin as shown in the circular pinhole to the left of Figure 2(b).

During implant, the wafer is in constant contact with the grounding pin to ensure proper dissipation of the accrued charge. Throughout the implant process, positive He+/He++ ions are targeted at the wafer resulting in positive charges accumulating on the surface of the photoresist and conducting metal surface. However, these metal contacts are encapsulated by the nitride and photo resist films with no means for excess charges to dissipate. The only path for this charge build-up to be released is through the grounded and un-insulated cross pattern and outer ring of the ESC chuck. This naturally increases the concentration of charges on the wafer metal features along the cross pattern and outer ring areas resulting in higher probabilities of ESD damage in those regions. This failure mechanism is illustrated in Figure 3 and explains the locations of the yield loss as well as the numbers of finding from the experiments mentioned above.

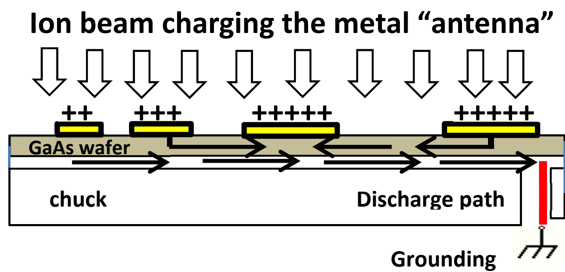


Figure 3. Illustration of the charge distribution across the wafer during implantation and the dissipation path through the grounded channels of the ESC chuck.

Specifically, this theory supports the observation that higher implant beam currents will result in higher amount of charge bombarding the wafer which then becomes congested around the grounding regions during implant and subsequently leads to higher ESD failures. In addition, this would suggest a direct relationship between the exposed metal surface area on the wafer during implant and the yield impact due to ESD damage. With ESD being dependent on the size of the contact area, this would account for the commonly observed defect map where the smaller, isolated transistors are unaffected by ESD while the larger arrays of HBT are more prone to the effects of electrical discharge as evidenced in the optical inspection yield map in Figure 4.

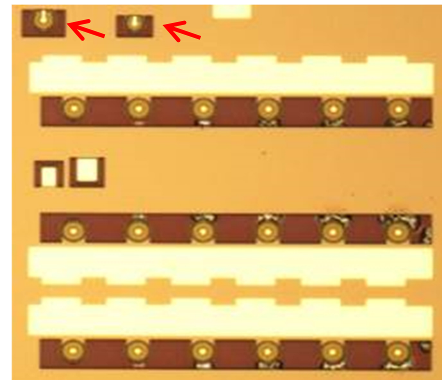


Figure 4. ESD defects on HBT transistor array and lone transistor without ESD failure.

CONTAINMENT AND RESOLUTION

One industry-established method in addressing implant-related ESD damage is to incorporate an electron shower (E-shower) capability into the implant process [1]. This additional filament integrated into the hardware essentially floods the ion beam with a surge of negative charge that neutralizes the positive He+/He++ ions prior to implantation as displayed in Figure 5.

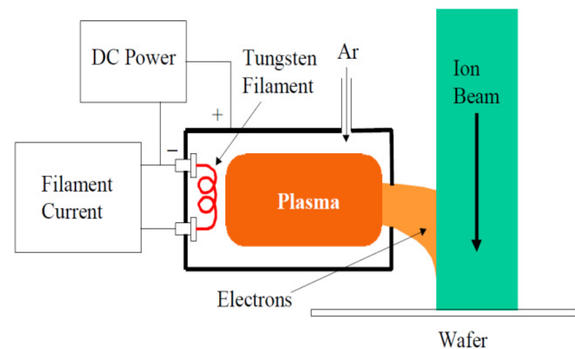


Figure 5. Diagram of the Implanter with E-Shower.

Although this is undoubtedly a dependable solution, there are additional risks involved with implementing the E-shower and requires careful process development in optimizing the E-shower current settings. Establishing the proper E-shower current is essential to avoid inducing ESD damage with a surplus of negative charges. In this case, the solution can inadvertently cause the problem. Therefore, it is necessary to carefully balance the need for neutralization without having excessive charges that can also cause similar ESD issues.

To simulate an extreme ESD-prone condition, GaAs wafers were deposited with contact metal then coated with a blanket sheet of photo resist followed by a coat of Silicon Nitride. These wafers were then implanted with and without the E-shower beam enabled and the results are displayed in Figure 5. Wafer processed with E-shower showed no symptom of ESD in comparison to the non E-shower wafer exhibiting an extreme case of ESD damage.

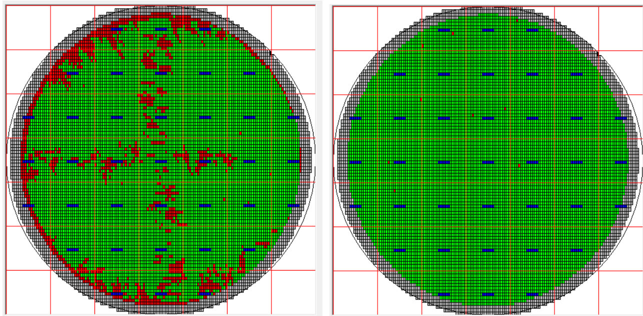


Figure 6. Yield maps of wafers without and with E-Shower during implant.

After iterations of Design of Experiment (DOE), the ideal E-shower process conditions were determined for the EATON/Axcelis 8250 implanter which allow for optimal isolation, cycle time and major improvement to the ESD yield loss. As with any tool upgrade, however, this can be a costly undertaking and in the present state of lean manufacturing, equipment modification is not commonly feasible. Therefore, alternative process methods are generally developed to mitigate and contain these types of yield loss. In this instance, one approach that was explored was reducing the implant beam current which ultimately limits the density of charge striking the wafer and thus decreasing the amount of charge collected at the contact metal in the cross-ring region. As expected, the level of the ESD damage is consistent with the magnitude of the implant beam current which is summarized in Figure 7 depicting a beam current DOE for a given implant process. In this experiment, the implant beam current was varied between 50% and 100%. The resulting implanted wafers were inspected immediately after implant on the August inspection tool and the number of ESD failure was compared against all defects that were detected. There was clear correlation between the beam setting and the amount of ESD loss. The degree of charging on the wafer as a function of the implant current was thoroughly studied by the EATON Corporation which first developed the E-shower capability back in the 1980's [1].

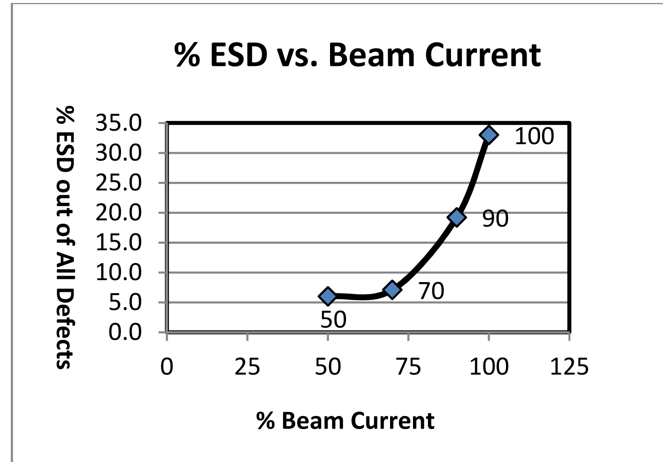


Figure 7. Plot of the % ESD damage out of all visual defects versus the implanter beam current for a given isolation recipe.

Another potential solution, although at times challenging is to redesign the layout of the device structures to isolate them electrically, keeping the overall surface area to a minimum and reducing the probability of charge build up on metal contacts which in turn can result in ESD. An example for this layout is showed in Figure 8 in which the transistors in the array are disconnected electrically and with smaller conducting surfaces, will acquire less charge and therefore less opportunities of an electrical discharge. This change can be implemented through etch, isolation process or altering the subsequent interconnecting metal.

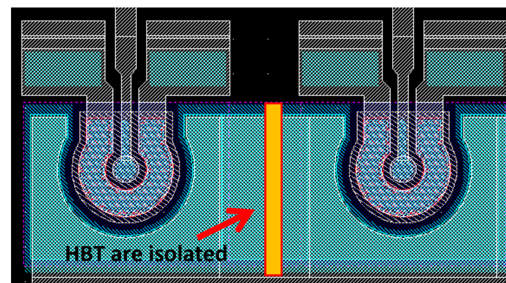
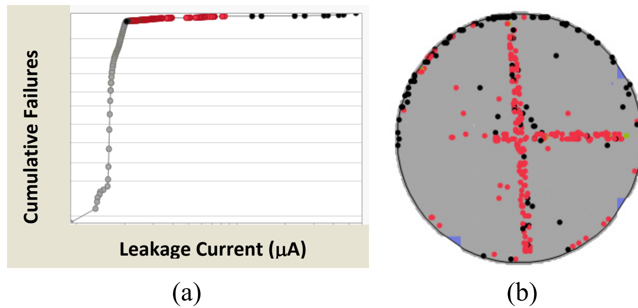


Figure 8. Layout showing the HBT segments are disconnected which help reduce charge buildup along the metal surface.

Finally, to further prevent additional escapes, a combination of visual inspection and probe test were implemented. Particularly, 100% final outgoing August inspection was used to screen out visual ESD failures while a special leakage test was applied to the standard functional probe test in order to catch any weakened die that might

have gone undetected. This test involved increasing the bias voltage in order to catch marginal or leaky dies. The failures uncovered by this method were later confirmed to be ESD induced which proved that this test is a good filter for this type of defects. Figure 9 depicts the leakage failure and resulting failed dies which again followed the cross and outer ring pattern consistent with the implant ESD damage.



(a) (b)

Figure 9(a) Example of extra leakage test detecting ESD failures (b) Yield map showing failed dies in the cross and ring pattern.

CONCLUSIONS

Through detailed assessment of the implant ESD failures, a better understanding of the cause and effect was determined. Subsequent root cause analysis helped establish ways of detecting and managing this yield issue. Although lowering the implant beam current considerably decreased the effect of ESD, it is not a practical solution with unfavorable impact to production throughput and can mostly serve as method of containment. Ultimately, the recommended solution would be to implement design and process flow protocols that limit the amount of conducting surface on the wafers prior to implantation. If these restrictions are not feasible, then the E-shower would be the best alternative. This is a well-established solution that can easily be incorporated into the existing implant process and with optimized process controls, allow for high yielding, reliable implant wafers while still maintaining a high beam current and excellent throughput.

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ACRONYMS

GaAs: Gallium Arsenide
HBT: Heterojunction Bipolar Transistor
ESD: Electro Static Discharge
ESC: Electro Static Chuck
DOE: Design of Experiment