Systematic Data Mining Methodologies for Yield Improvement

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Abstract

Investigating the root cause of electrical Die Sort (DS) yield loss is very time consuming and often becomes a frustrating task in a high-volume semiconductor manufacturing environment. Applying the right strategies will help yield engineers quickly narrow down the numerous potential interactions and help lead the integration and process teams to root cause identification, problem closure, and ultimately, future prevention. This paper will address how to effectively perform systematic drill-down analysis with case studies demonstrating yield improvement on products produced at Qorvo.

INTRODUCTION

In a high-volume semiconductor manufacturing fab, yield engineers fight with yield issues every day. Quickly identifying the origin of yield loss, is a key element in a company's success. Systematic data mining (also called knowledge discovery from data) was proven to be an efficient approach to manipulate the large set of data and further narrow down to the origin of yield loss. Data mining differs from standard data analysis where data analysis is usually used to prove or disprove a hypothesis. Data mining finds relationships in large sets of data that can lead to knowledge discovery [1]. The knowledge obtained from data mining, is just the first step in peeling off layers of the yield onion. Further validation through experimentation and failure analysis, needs to be performed to explain the failure mechanism physically and implement corrective actions accordingly.

In this paper, the systematic drill-down analysis developed at the Qorvo Hillsboro fab, will be described. The power of this drill-down technique will be demonstrated through real-world successful case studies, starting from problem identification and ending ultimately in yield improvement.

SYSTEMATIC DATA MINING PROCEDURES

1. Population Selection and Data Prerequisite

When electrical test yield turns unexpectedly lower, there is often an associated turn-on date. To capture trends as a function of time, data mining should always cover a date range, including both periods of historical (or baseline) and abnormal yields. Fig. 1 illustrates an example from a timestamp when the die sort yield loss deviated from a normal baseline.

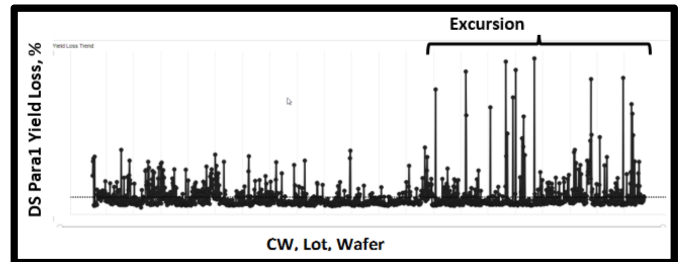


Fig. 1. DS Yield Loss Trend Ordered by Calendar Week, Fab Lot, and WaferID

Besides determining what population to include for analysis, a critical step is to make sure that the following datasets for each lot and wafer, are collected and considered a minimum at Qorvo:

- Overall DS yield, individual test yield data for each wafer and the raw measurement results for each die
- Process Control Monitor (PCM) raw data from each wafer and wafer aggregation data for each test parameter
- Fab tool history (i.e. Tool information on the material as it was processed at each fabrication step and timestamp)

Qorvo utilizes an internally developed Spotfire (TBICO®) [2] drill-down dashboard. The dashboard allows users to automatically retrieve DS, PCM, and tool history data given a specific product over a desired period. It has saved yield engineers significant time through automatically preparing data, performing correlations and visualizations efficiently through the built-in analysis template. Furthermore, it makes the drill-down process with a large

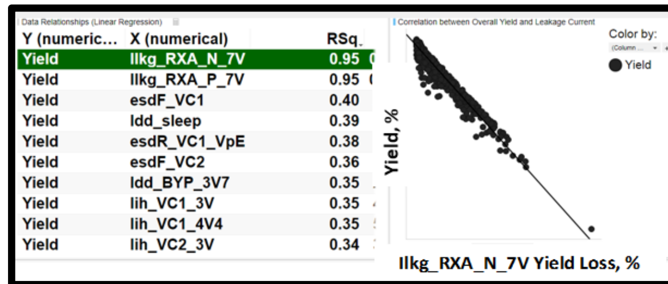
amount of available data, very quick and shortens the loop for solving yield loss. It also helps identify parametric trends, hopefully before yield losses can begin.

2. Yield Loss Pareto

A typical DC test battery at die sort is part of the standard fabrication process, which allows the die to be characterized not only the electrical performance, but also to ensure high product yield, low defect levels, and long-term reliability. It is also called identifying Known Good Die (KGD). The test program varies from product to product. In general, when overall DS yield decreases, it is usually driven by a specific parameter. Understanding the driving force for yield loss is the fundamental step for root cause investigation. Qorvo employs three methodologies to identify the dominant yield detractors as described below.

- **Correlate Overall DS Yield with Individual Test Yield**

Spotfire has a built-in feature allowing the user to perform linear correlations and display the results, sorted in order from strongest to weakest by R-squared. As shown in Fig.2, the correlation ranking guides the focus of the investigation on specific parameters that might be influencing yield loss the most.



Y (numeric...	X (numerical)	RSq
Yield	Ilkg_RXA_N_7V	0.95
Yield	Ilkg_RXA_P_7V	0.95
Yield	esdF_VC1	0.40
Yield	Idd_sleep	0.39
Yield	esdR_VC1_VpE	0.38
Yield	esdF_VC2	0.36
Yield	Idd_BYP_3V7	0.35
Yield	Iih_VC1_3V	0.35
Yield	Iih_VC1_4V4	0.35
Yield	Iih_VC2_3V	0.34

Fig. 2. Correlation between Overall DS Yield and Individual DS Parameters

- **Pseudo Yield Loss Pareto**

This strategy only considers the overall average failure rate on each DS parameter and neglects the cases where the specific die fails for multiple related tests and that is why it is called 'Pseudo Yield Loss'. As shown in Fig. 3, almost 80% of the yield problems could be resolved using pseudo yield loss pareto by focusing on the dominant detractors.

- **Real Yield Loss Pareto**

It is a deep drill-down to sort the die by specific failure modes or combination of many. Spotfire allows the characterization of the failure modes (including failing lower SPEC limit or higher SPEC limit specifically) of each die. This approach is very helpful to identify the true failure mechanism by isolating the issue from other potentially unrelated failure mechanisms. Fig. 4 demonstrates the example where shorted capacitors failed capacitor leakage parameters predominantly, but didn't fail for other parameters, i.e. the top bar for failing both cap leakage and stress tests.

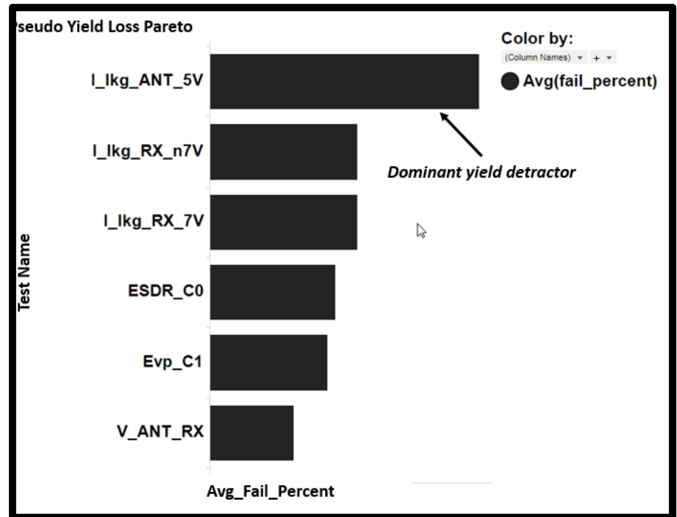


Fig. 3. Pseudo DS Yield Loss Pareto

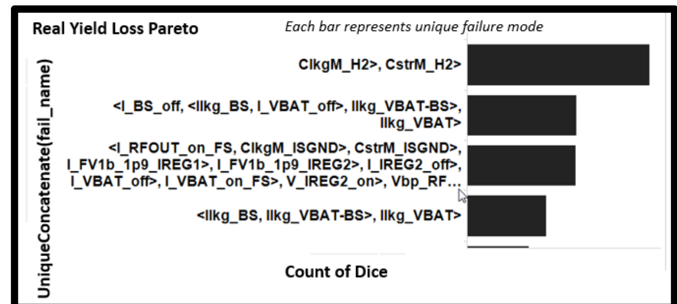


Fig. 4. Real Yield Loss Pareto to Identify Cap Leakage

Each approach has its own advantage and disadvantage. Yield engineer judges, on a case-by-case basis, which approach is best to use for a given problem.

3. Wafer Level Correlation for Potential Root Cause

Upon identifying the dominant DS yield detractor, the next step is to drill down what could cause the issue potentially. Every fab has Process Control Module designed on each product to monitor the health of process steps closely, therefore an efficient way is to correlate DS yield change with PCM data. A Qorvo-developed ZONAL approach was presented at Mantech in 2017 [3]. The ZONAL technique is a very powerful tool, but not applicable to daily data analysis, as it needs more time to identify the ZONAL dice and transform the coordinates from the DS coordinate map into PCM map. It is very helpful for new failure modes or evaluating test correlations on products in development or pre-production release windows.

Instead of employing the ZONAL technique, finding correlation using wafer-level aggregation data, is an efficient way to determine the potential contributors. Yield loss or wafer-level aggregation on specific DS parameters can be joined with PCM data. Once the combined data set is configured, correlation analysis can be easily performed by Spotfire. This step was also built into the dashboard.

The following section will apply the data mining methods, discussed in the previous sections, to actual yield improvement encountered at Qorvo.

CASE STUDIES

CASE 1 – DS Yield Loss Driven by Photo Scumming

As shown in Fig. 1, DS yield loss on test Idd_BYP_3V7 was elevated and consistently showed up at the edge of the wafer with photo print field tile-pattern as shown in Fig. 5. Both visual inspection under an optical microscope and failure analysis, confirmed that the failing dice were caused by missing transistor gate metal. In the meantime, the fab experienced a process excursion, which led to wafer scrap caused by scumming within features at a photo layer. At the start of the excursion, a focus team was formulated and had the following findings:

- Inline wafer scrap was unnecessary. DS testing was able to catch the failure and screen the failing dice out. This was a significant finding and confirmation to prevent wafers from being scrapped inline and thusly maintained high inline wafer yield.
- For the wafers impacted by scumming, specific PCM test data also showed spikes at sites adjacent to the edge of wafer as shown in Fig. 6., which also allowed the team to find inline correlation and have the ability to evaluate any process changes at an earlier test point.
- Further investigation proved that the root cause for scumming was driven by thinner wafers. The thickness uniformity issue made the stepper focus marginal, which created scumming, which is under developed / exposed photo resist in the open gate features. Split experiments have confirmed the model that thinner wafers caused the issue and indicated a potential turn on date at the substrate supplier. A continuous improvement project is being worked on between Qorvo and wafer substrate supplier.

CASE 2 – DS Yield Loss Driven by VpE uniformity

In a family of pHEMT products, a consistent DS yield loss is observed in the form of leakage currents (dominant detractor in yield loss pareto). The failure pattern is illustrated in Fig. 7 and is prevalent at the 1 O'clock to 3 O'clock positions (i.e. dark area).

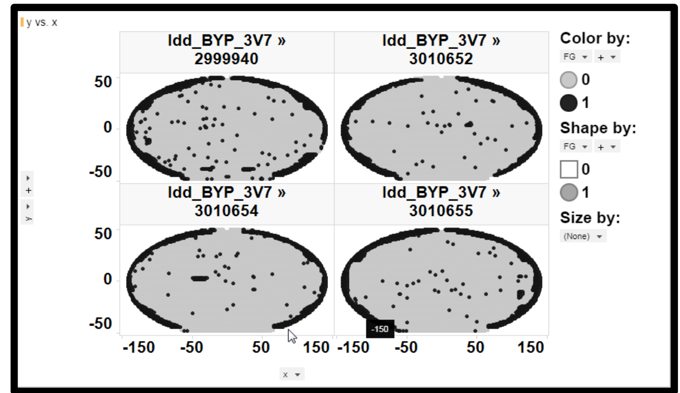


Fig. 5. Failure Pattern on Idd_BYP_3V7 Yield Loss (edge of wafer)

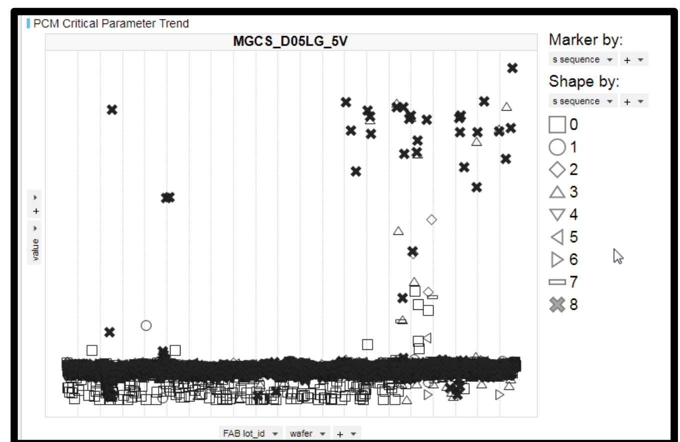


Fig. 6. PCM Signals Correlating to DS Yield Loss at Edge of Wafer (s sequence=8 represents 3 o'clock PCM)

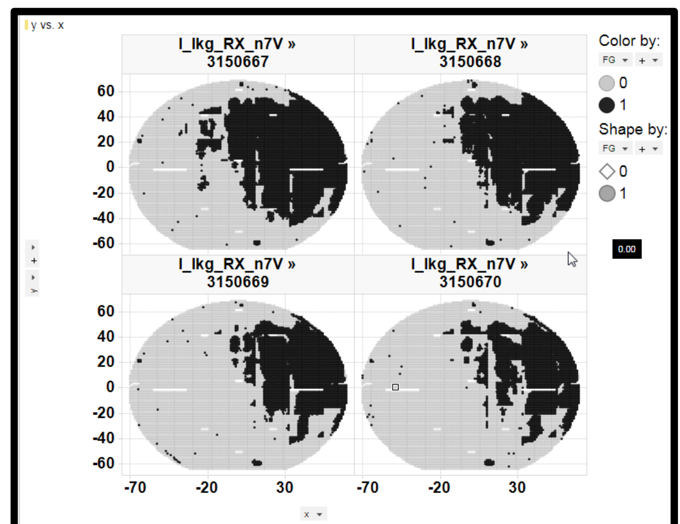


Fig. 7. Failure Pattern on Leakage Current for Case 2

Through systematic data mining methodology and applying the ZONAL technique, it was found that the leakage current (I_lkg_RX_n7V) yield loss was strongly correlated to more negative EFET Vp as shown in Fig. 8. Further drill-down analysis identified within wafer non-uniformity patterns on EFET Vp, specifically near the 3 o'clock PCM site, see Fig. 9. Based on this analysis, an integrated module team (IMT) was formulated and root cause investigations were initiated. The preliminary experiment showed that intentional expansion at photo could potentially improve EFET Vp uniformity as illustrated in Fig.10 with very promising results (40% improvement on EFET Vp uniformity and 20% improvement on DS yield).

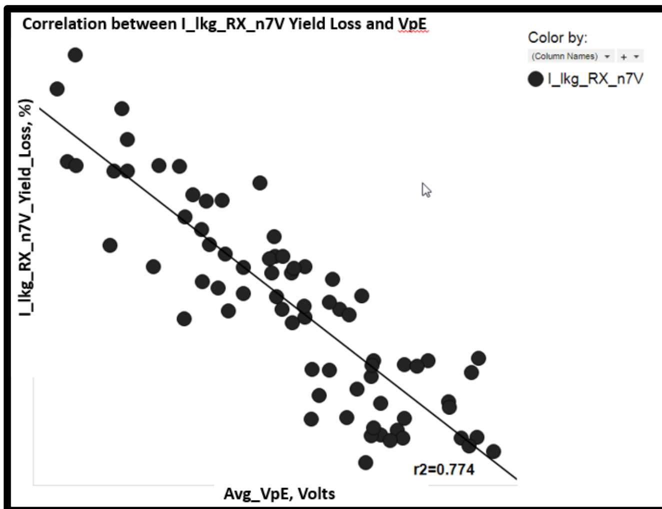


Fig. 8. Correlation between I_lkg_RX_n7V Yield Loss and EFET Vp by Wafer Average

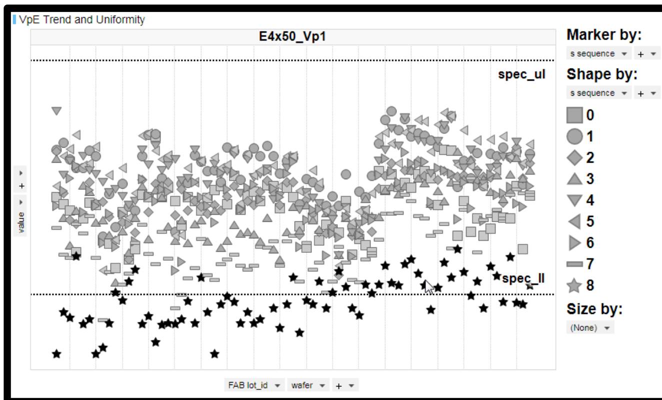


Fig. 9. EFET Vp Uniformity (s sequence=8 represents 3 o'clock PCM site)

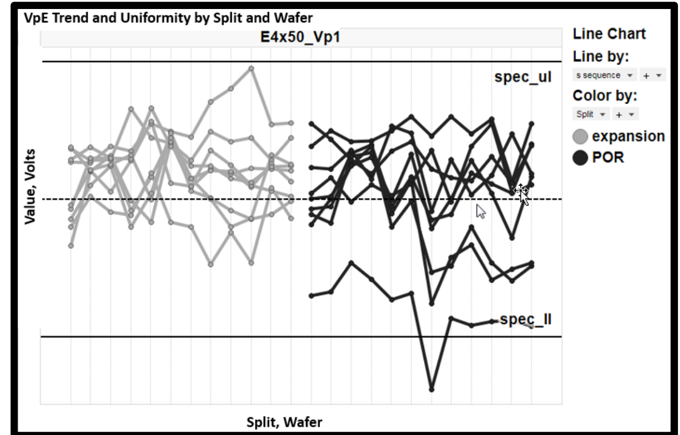


Fig. 10. EFET Vp Variation Comparison between Intentional Expansion and POR

CONCLUSIONS

Applying the right approach to perform yield analysis is critical to identify the potential contributors quickly, and further guide the team in the right direction. Consistently performing systematic analysis would enable continuous yield improvement and make significant cost savings for the company and further lead to an increase in productivity.

REFERENCES

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ACKNOWLEDGEMENTS

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ACRONYMS

DS: Die Sort
PCM: Process Control Module
KGD: Known Good Die
pHEMT: Pseudomorphic high-electron mobility transistor
VpE: Threshold Voltage at Enhancement Mode
IMT: Integrated Module Team
FA: Failure Analysis
MGCS: Multiple Gate Current Source
ZONAL: Zone Analysis