Plating Defect Detection and Process Control

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Abstract

Electroplating Au interconnect metal on a non-planar process has unique process control challenges. In this work, we analyze Au plating problems for a non-planar GaAs process for high power applications and demonstrate improved process control.

INTRODUCTION

Electroplated Au interconnects are commonly used in III-V backend processes. Typically, the thickness of electroplated layers are > 2μm whereas thinner Au interconnect layers are usually processed using liftoff. The electroplated Au process begins by sputtering a seed layer across the surface of the wafer. The seed layer usually consists of an adhesive metal layer (Ti is common for use in this application) followed by Au. Once the seed layer is sputtered, photoresist is deposited and patterned across the wafer. With the pattern on the Au seed wafer surface, the wafer can be Au electroplated on its surface to the desired thickness [1]. After the final metal deposition, the resist is stripped and the seed layer removed from the wafer surface where the Au was not plated. Problems that can occur from this series of processes include resist pattern defects and plating seed metal that is not removed (or residue). The process monitoring of this process will be demonstrated along with complications that arise with plating metal on a conformal/non-planar process.

Defects associated with Au plating processes include high leakage currents caused by seed removal failure, photo pattern defects, high metal surface roughness, and metal thickness variation. For IPD processes, plating defects can lead to shorting, reduced capacitor ruggedness, and undesirable impedance shifts in matching applications. Such defects can be even more acute when the IPD is used as matching circuit in a high power, non-mobile application.

Leakage current and seed removal can be monitored with DC testing along with inspection [2]. On many occasions high leakage currents measured during DC monitor testing also show signs of seed removal problems upon visual inspection. Figures 1 and 2 show leakage test structures used to detect plating seed where the horizontal lines represent the plated Au metal (metal 3) in the process. It was later determined that added topology underneath the plated Au layer reducing the planarity of the surface would affect the ability to remove the plating seed. This resulted in the development of the structure in Figure 2 which simulates an inductor cross-over. The SEM of both structures are shown in Figures 3 and 4.

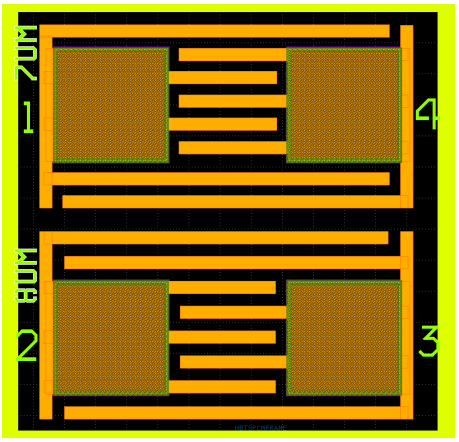

Fig.1 Comb structure used to measure leakage between horizontal plated Au lines on planar surface (no underneath topology)

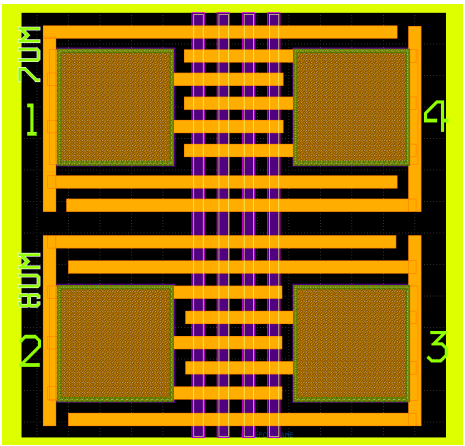

Fig.2 Comb structure used to measure leakage between horizontal plated Au lines on top of vertical M1+M2 lines

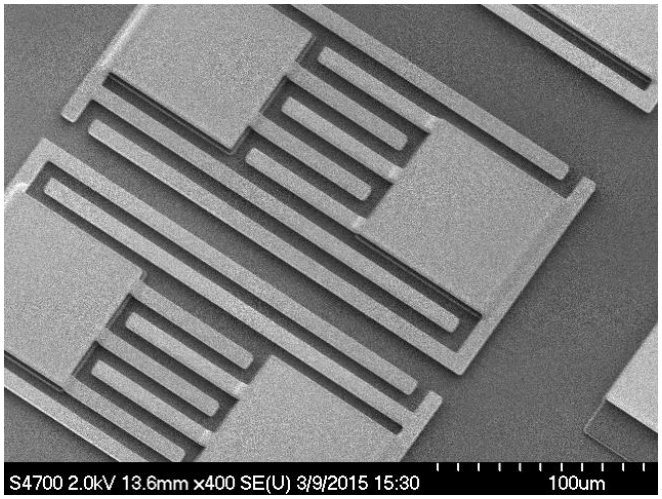

Fig. 3 Planar comb structure from Figure 1 used to measure leakage between horizontal plated Au lines

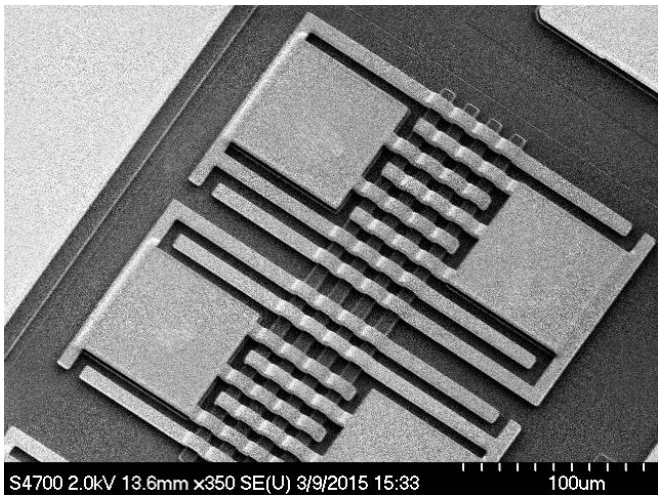

Fig. 4 Non-planar comb structure from Figure 2 used to measure leakage between horizontal plated Au lines on top of vertical M1+M2 lines

The test structures are placed across the wafer to look closer into the process variation. High voltage (HV) DC testing is performed in an automated testing environment. Sampling is optimized to capture any process variation while minimize the test time. Multiple sites are usually measured across the wafer.

The test structures are tested by placing high voltages across them and measuring the leakage current. A high leakage current or early breakdown could be a result of a plating-related defect within the test structure. A defect seen or measured on a structure like in Figure 4 could also mean product failures could occur on devices with similar topology like an inductor crossover as seen in Figure 5. However, the same failure seen on the non-planar comb Figure 4 may not be seen on the planar comb in Figure 3.

In-line monitoring of the photoresist thickness can reduce the risk of formation of the plating profile defect shown in Figure 6. Also, this type of defect can be detected with DC PCM testing on the comb structure [3,4]. Leakage current would be elevated due to a small spacing between metal lines.

To monitor sheet resistance, the plated metal Van der Pauw style-method can be used (Figure 8).

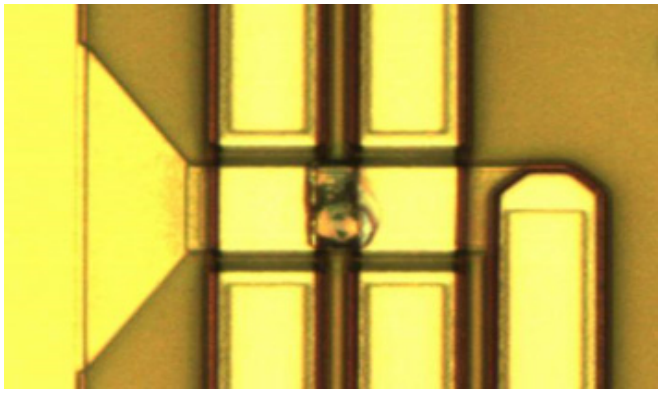

Fig. 5 Inductor failure after high power stress due to un-etched plating seed

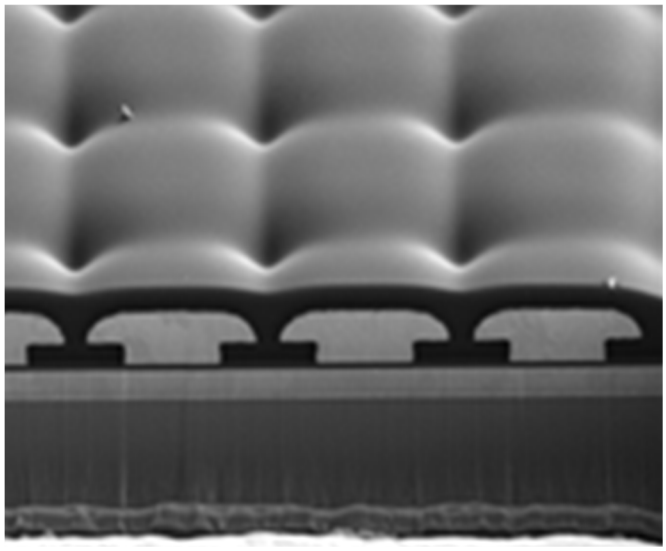

Fig. 6 Plating defects due to photoresist thickness variation

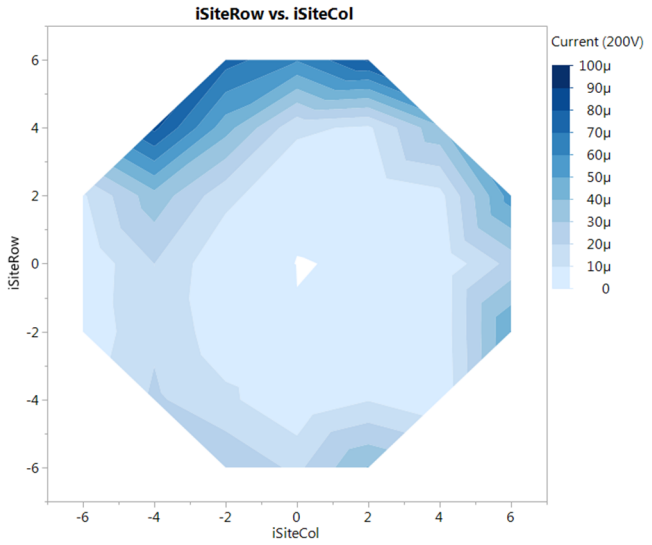

Fig. 7 Abnormal leakage measured on comb structure was a result of the plating-related defects.

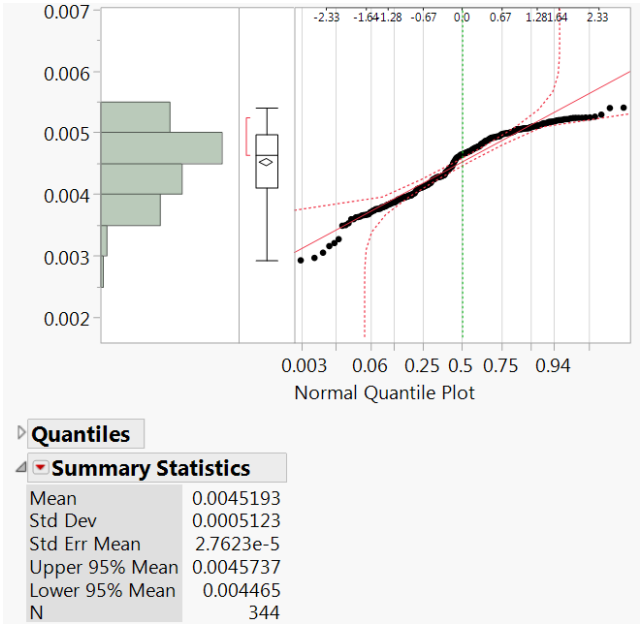

Fig. 8 Sheet resistance (R_{SH}) measured across the wafer.

Process control can be used to improve existing processes. Using the leakage detection structures described previously, processes such as the wet etch tank life and the plating bath life can be studied to determine effects over time. Figures 9 and 10 show the reduced leakage outliers after changing out a wet etch tank solution. The result of this experiment demonstrates that the wet etch tank life can affect the IPD die yield and die performance.

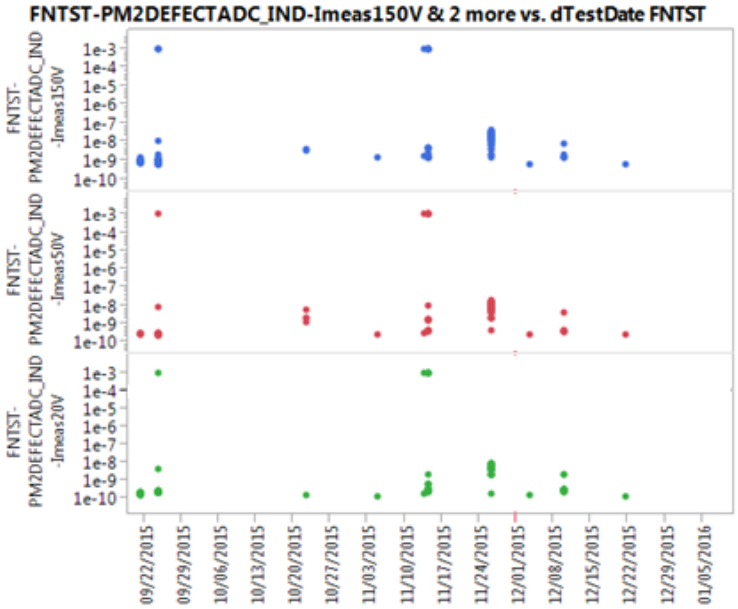

Fig. 9 Leakage current of comb structures shown over the life of an unchanged Au etch tank.

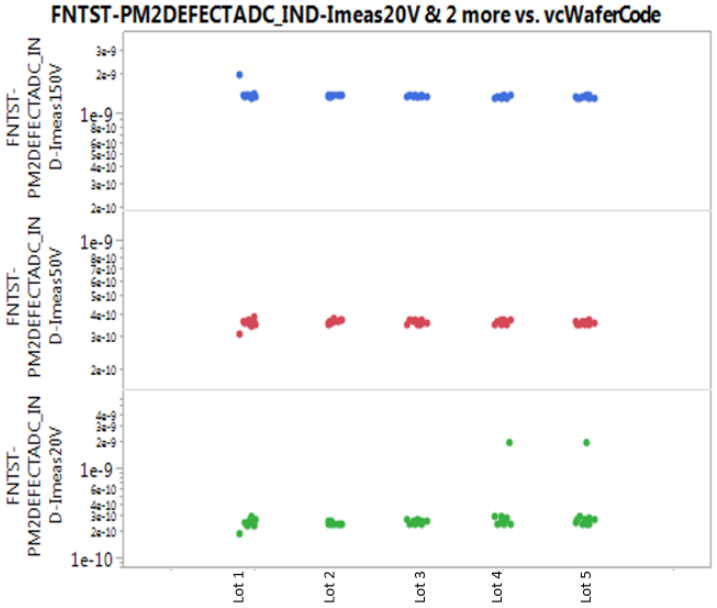

Fig.10 Leakage current of comb structures of first five lots after replacing Au etch tank described in Figure 9.

Even though DC process control can be effective in detecting a widespread issue across the entire wafer, product or die sort testing can improve detection where issues may be more localized. Die sort testing for this application may involve using high DC voltages to measure leakage between passive devices such as capacitors, inductors, or between areas of the circuit that may impact performance. The high voltages may be needed to detect minor amounts of plating seed defects which may affect performance and/or reliability.

SUMMARY AND CONCLUSIONS

Plating defects can be monitored with inspection and DC testing. The DC biasing of the PCM structures should reflect the biasing magnitudes seen on the product devices which may be high power. It is possible for such defects to occur where planarity is minimal. Novel test structures may be needed for process control for non-planar processes. Subtle seed residue can cause failures in high power applications. Inspection can consist of either visual inspection or AOI. Inspection may help determine the cause of defect, but it should complement DC testing since a plating related problem may be difficult to detect optically.

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ACRONYMS

MIM capacitor: Metal-Insulator-Metal Capacitor
IPD: Integrated Passive Device
PCM: Process Control Monitor
HV: High Voltage
AOI: Automated Optical Inspection
Ti: Titanium
Au: Gold