Device-to-device coupling via lateral conduction within the epitaxy in C-doped AlGaN/GaN-on-Si HEMTs

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Abstract – Carbon doped AlGaN/GaN power switching devices can show parasitic lateral leakage within the epitaxial layer. Here we demonstrate that lateral leakage occurs outside the active area of the device resulting in device-size-dependent back-gating effects and cross coupling to adjacent devices. This can result in time dependent changes in on-resistance in devices located more than a millimeter away from the active device. We also show that the lateral leakage path is highly non-ohmic, displaying an unusual oscillatory relaxation process.

I. INTRODUCTION

AlGaN/GaN based HEMTs are finding increasing application in high-power and high-frequency systems. Considerable effort has been put recently into buffer design and understanding different conduction mechanisms since they impact breakdown and current collapse. Dopants like carbon (C) havebeen widely used to improve lateral and vertical breakdown strength but have resulted in charge trapping in the buffer, leading to issues like time dependent ON-resistance (Dynamic R_{ON}) and current collapse (CC). Surface trapping has been resolved mostly with good passivation techniques and better field plate design, but bulk trapping has been an ongoing problem affecting long term stability of these devices. Hence it is important to understand charge flow in the different layers and interfaces for different doped buffers [1-3]. In particular,it has previously been shown that charge can flow laterally within the buffer outside the active area of the transistor resulting in an area dependent sensitivity to substrate bias [4, 5].

In this work, we show that this lateral leakage can result in cross-coupling between devices and buffer induced negative dynamic R_{ON} in adjacent devices for carbon doped buffer. We also demonstrate that the lateral transport process outside the active area is highly non-linear. Using substrate bias method we demonstrate lateral spreading up to 2mm wide and the impact on the device performance. We also observed very unusual step-like "ripples" indicating a form of a repetitive relaxation process. It is important to understand the charge storage and lateral flow mechanisms within the epitaxy to be able to utilize them wisely for applications such as integrated drivers which demand that active devices share the same die. It also may impact on-wafer reliability investigations since device probing can result in changes to unpowered adjacent devices.

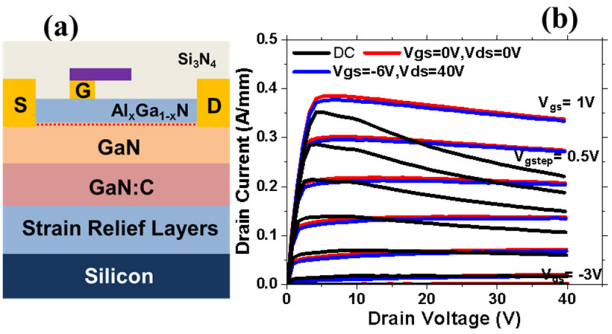

Fig. 1 (a) Generic cross section of the carbon doped GaN-on-Si HEMT structure **(b)** Output DC and Pulse I-V measurements with 1µs pulse length and 1ms pulse period at different gate and drain stress biases showing minimal knee walkout.

II. RESULTS AND DISSCUSION

The samples used in this study are grown using MOCVD on p-type Si substrate, consisting of a conventional stack of AlN nucleation layer, superlattice buffer, carbon doped GaN, unintentionally doped (UID) GaN channel, and AlGaN barrier. The generic structure is shown in Fig. 1a. The HEMT devices were fabricated using mesa isolation, Ti-Al-Ni-Au Ohmic contacts, Ni-Au Schottky gate and Si_3N_4 passivation. Single finger transistor with width Wg=100µm, gate length Lg=1.5µm, source to gate distance Lsg=2.5µm and gate drain spacing Lgd=12µm has been used. DC output characteristics showed Ids of 200mA/mm, with threshold voltage measured at -2V and off state leakage in the order of 10^{-9}A/mm. Pulse measurements with 1µs pulse length and 1ms period have been used to monitor surface and buffer trapping effects with different stress conditions of Vgs=0V, Vds=0V (no stress), Vgs=-6V and Vds=0V (probing the area near the gate) and Vgs=-6V and Vds=40V (gate and drain access region). No significant knee walkout, Vth shift or gm collapse were observed as shown in Fig.1b, indicating good surface and buffer qualities.

Substrate bias sweeps were performed to study charge trapping and transport in the buffer [6, 7]. Monitoring the channel conductivity upon substrate bias sweep and its dispersion at different ramp-rate and temperature allows one to explain transport within each layer in the buffer. The technique is normally surface insensitive, i.e. enables selective access to the effect of buffer on device performance and has been used to understand charge storage primarily in the buffer. Back-bias on a large area TLM contact is shown in Fig.2, and as the substrate bias

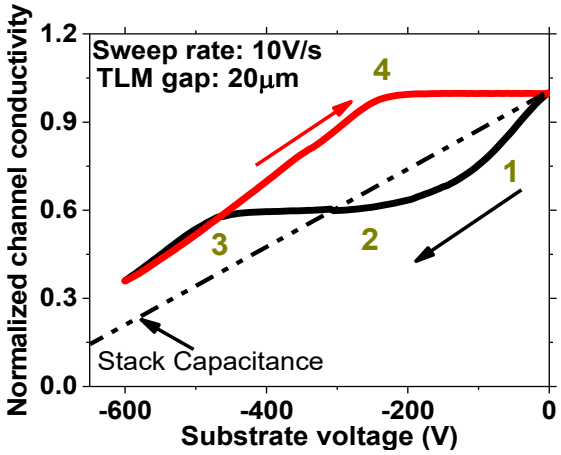

Fig. 2 shows the normalized channel conductivity of a large TLM structure as substrate bias is swept up to -600V and back to 0V with 10V/sec sweep rate, the black dotted line represents the stack capacitance.

is varied, a combination of vertical and lateral leakage and charge redistribution leads to deviations from the capacitive line corresponding to the predicted response if the buffer stack were a perfect dielectric. The behavior is entirely consistent with that observed with high quality epitaxy [3, 5]. It shows localized hole charge flow within the GaN:C layer (Region 1), onset of leakage through the UID GaN layer and positive charge storage (Region 2), onset of leakage through the SRL (Region 3), and forward biasing of the 2DEG to buffer junction injecting electrons (Region 4). The key observation is that after ramping back to Vsub=0V, there is no change in channel conductivity indicating no net buffer charge and no significant dynamic Ron.

The initial drop (Region 1, 2) has been further studied by performing back-bias measurements on devices with different active mesa areas. As shown in Fig.3 we observe that the initial drop is strongly size dependent, with a magnitude in small devices that is too large to explain

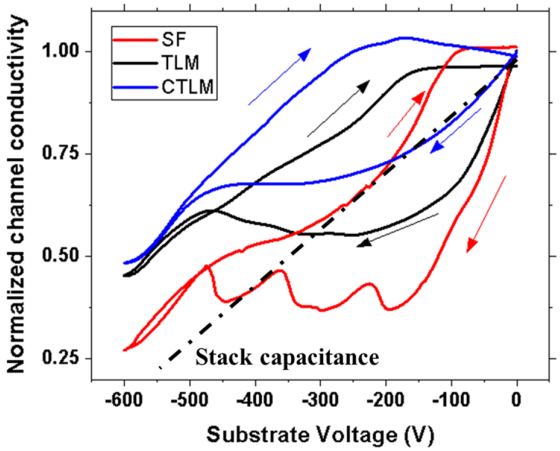

Fig. 3 – Normalized channel conductivity as a function of substrate voltage of 3 structures with different active areas: Single finger (SF of 9.10^{-3} mm^2), TLM (85.10^{-3} mm^2) and CTLM (384.10^{-3} mm^2).

using 1D models of vertical charge redistribution within the buffer. This has previously been explained by hole charge flowing laterally within the buffer outside the active area defined in this case by the mesa [4, 5]. This lateral charge flow increases the effective size of the device, changes the vertical potential distribution through the stack, increases the electric field under the 2DEG, and reduces the channel current especially for small devices. The consequence is that measurement results obtained on small test devices will not necessarily apply directly to large power devices.

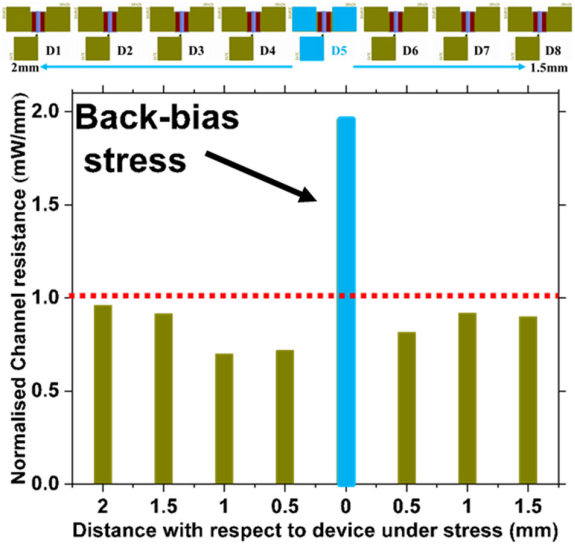

Fig 4. Normalised Channel resistivity with respect to initial value of 8 adjacent devices before and after stress. Stress is applied by sweeping the substrate up to -600V on the central device, and measurements were undertaken by repositioning probes taking about 2min. Device schematics are shown above.

The impact of lateral charge flow can be seen directly in Fig. 4, where the normalized change in channel resistance with respect to initial value is shown on 8 adjacent devices. The central device was substrate biased up to −600V and then stepped directly back to 0V, with probes only connected to the central device. Subsequently, manual repositioning of the probes to each adjacent device allowed the remeasurement of the channel resistance, with all the measurements taking about 2 minutes. There is clear coupling between devices, with unbiased adjacent transistors showing a decrease in R_{ON} of up to 45% (negative dynamic R_{ON}) enduring for minutes, as compared to an increase in R_{ON} on the biased central device. The spacing between the devices, each having independent mesa, is about 400µm, thus the device-to-device coupling extends up to about 2mm. The sign of the change in R_{ON} in the adjacent devices is fully consistent with a model where the current is flowing laterally within the bulk of the buffer as shown in Fig. 5 [5]. The key element of this model is that the GaN:C layer is more conductive than the UID GaN or SRL layers. So, with substrate-bias of −600V, there is a voltage drop

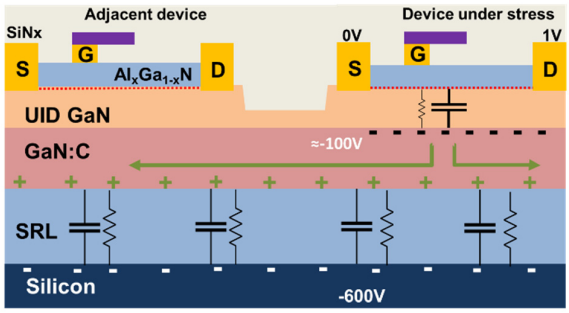

Fig. 5 – Schematic shows negative charge build-up under device stressed (increase in R_{ON}) and voltage drop across SRL leading to spread of positive charge under adjacent devices (decrease in R_{ON}).

across the UID GaN layer under the central device which leads to an accumulation of negative charge close to 2DEG resulting in an increase in R_{ON}. Lateral conduction in the GaN:C layer under adjacent devices produces the device-to-device coupling. There the voltage drop across the SRL results in a positive charge and hence a decrease of R_{ON}. Surface leakage can be discounted as a mechanism since it would have resulted in an increase in RON in adjacent devices due to a voltage dropping across the UID GaN layer under those devices, as happens for the central device [3]. This lateral conduction mechanism could have a significant impact during on-wafer reliability characterization since it creates lateral leakage within the buffer leading to charge accumulation and hence cross-coupling between devices, requiring careful consideration of the prior measurement history of adjacent structures on a wafer.

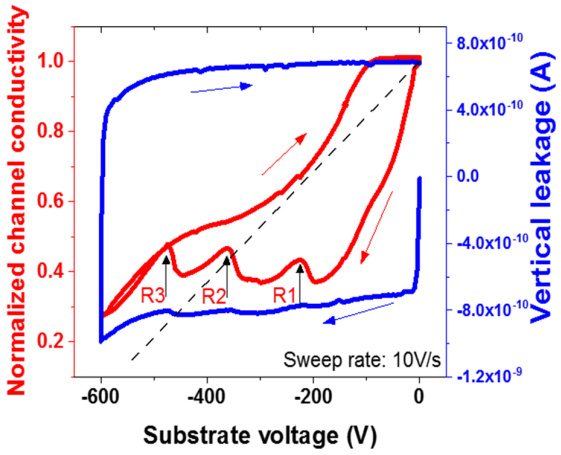

Fig.6 Normalized channel conductivity and vertical leakage of a single finger transistor exhibiting ripples.

Fig. 6 shows the normalized channel conductivity and the vertical leakage as a function of the substrate voltage on a single finger transistor as the Si substrate is ramped at 10V/s. The highly unusual result found here is the "ripples" (labelled as R1, R2 and R3). These are seen in all devices fabricated on this epitaxy and were reproduced in two separate device runs. The ripples appear at the same voltages in all similar devices and are most visible in the smallest devices. They are also weakly visible in the substrate current, which is primarily a capacitive charging current, and not a leakage, as demonstrated by the fact that it reverses for the backward sweep. The voltage at which the ripples appear is dependent on ramp rate, with a larger spacing at higher rate. We note that the magnitude of the ripples remains the same for a given ramp rate, with a constant spacing in voltage. One possibility to explain this is that the transport is controlled by a relaxation oscillation in occupation of traps. Charge is stored locally until some critical density is reached at which it initiates a detrapping phase. The presence of an oscillation suggests some gain within the detrapping process; however its origin is unknown at present.

III. CONCLUSION

Lateral current flow is shown to occur within the carbon doped GaN-on-Si epitaxial buffer. The lateral leakage is occurring outside the active area of the device resulting in coupling to adjacent devices out to a distance of 2mm. This epitaxy mediated device-to-device coupling has important implications, especially for applications where multiple devices are integrated on the same die, such as integrated drivers for power FETs, and may also impact wafer probe results.

ACKNOWLEDGEMENTS

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