Performance and Stability of Enhancement-mode Fully-recessed GaN MIS-FETs and Partially-recessed MIS-HEMTs with PECVD-SiN_x/LPCVD-SiN_x Gate Dielectric

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Abstract

Characterizations were systematically conducted to compare the stability and reliability of the E-mode GaN-based fully recessed gate MIS-FETs and partially recessed MIS-HEMTs with the same gate scheme featuring PECVD-SiN_x/LPCVD-SiN_x dielectric stack. Despite a moderately larger R_{ON}, the MIS-FET delivers improved V_{TH} uniformity and thermal stability. Similar reduced long-term PBTI and enhanced stability under NBTI stress could be simultaneously obtained in the MIS-FET in contrast with the MIS-HEMT. The MIS-FET could also deliver superior V_{TH} stability under pulsed-mode gate bias characteristics compared with the MIS-HEMT. It is revealed that the electron trapping/de-trapping resulting in the instability difference occurs at both the dielectric/III-N interface and in the gate dielectric border.

INTRODUCTION

Owing to the highly desired enhancement-mode (E-mode) operation and the capability for providing large forward gate voltage swing [1], the GaN-based fully recessed gate MIS-FET and partially recessed MIS-HEMT are especially attractive for high-frequency power switching applications [2]. In addition to the enlarged gate swing and lower gate leakage, gate dielectric is also required to deliver high reliability and stability. The recently reported gate dielectric scheme of PECVD-SiN_x/LPCVD-SiN_x dielectric stack can deliver a high-quality dielectric/GaN interface, high breakdown electric field and long TDDB lifetime [4][5].

The MIS- gate structure, however, tends to introduce shallow and deep traps (with short and long emission time constant τ_{it}) at the dielectric/III-nitride interface or within the dielectric bulk. These traps could exchange carriers with the channel under forward or reverse gate bias stress, resulting in a gradual shift in V_{TH} and possible gate degradation. Although there have been extensive investigations focusing on instability and reliability in MIS-HEMTs and MIS-FETs, a systematic comparison between these two types of power devices with the same gate dielectric stack is still lacking.

In this work, such a comparative study was carried out by performing comprehensive device characterization. We

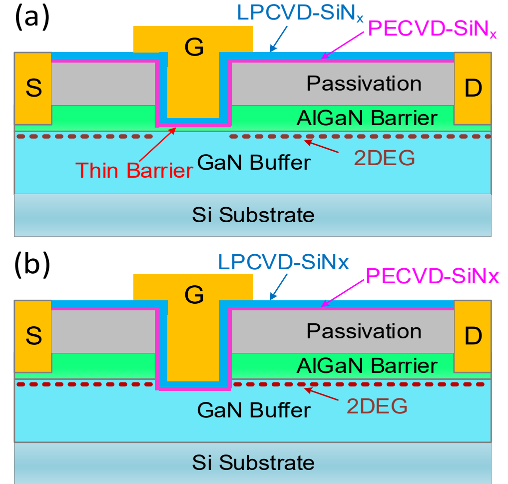

Fig.1. Cross-sectional schematic of (a) MIS-HEMT with partially recessed gate and (b) MIS-FET with fully recessed gate structure. Gate dielectric: PECVD-SiN_x/LPCVD-SiN_x.

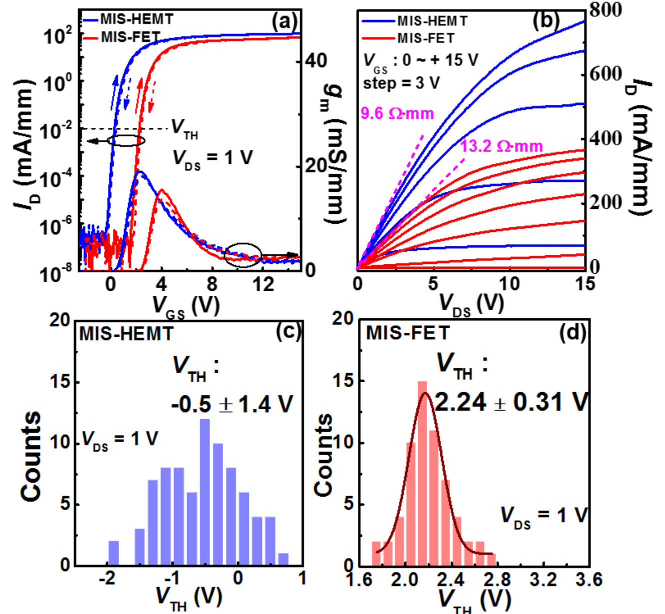

Fig. 2. DC (a) transfer, (b) output characteristics of MIS-HEMT and MIS-FET. Histograms of V_{TH} measured from (c) 50 MIS-HEMTs and (c) 50 MIS-FETs. V_{TH} is defined at 10 μA/mm (Device dimension: $L_{GS}/L_G/L_{GD}$ = 2/1.5/15 μm)

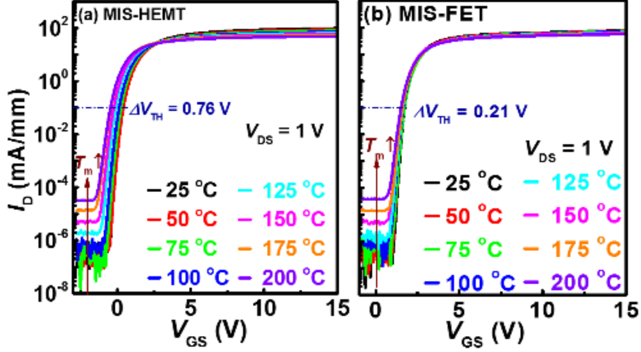

Fig. 3. Temperature-dependent transfer characteristics of (a) MIS-HEMT and (b) MIS-FET with measurement temperature (T_m) increasing from 25 °C to 200 °C. (Device dimension: $L_{GS}/L_G/L_{GD}$ = 2/1.5/15 μm).

revealed that thermally-induced V_{TH} shift is manifest in MIS-HEMT, but negligible in MIS-FET. We also investigated the positive/negative bias instability through both long-term bias stress and pulsed stress tests. We have demonstrated the highly stable V_{TH} and R_{ON} of both devices, with small PBTI but suppressed NBTI obtained in MIS-FETs. In addition, we specify the possible trapping/de-trapping process corresponding to these different behaviors between the two devices.

Device Structure and Characterization

The studied MIS-HEMTs and MIS-FETs were fabricated with previously reported process flow [5], except that the MIS-FETs feature a fully recessed gate while the MIS-HEMTs keep a ~2.6 nm thin AlGaN/AlN barrier layer above the heterojunction channel (Fig. 1). The gate dielectric stack consists of a ~2 nm PECVD-SiN_x protection layer prepared at 300°C followed by an LPCVD SiN_x layer deposited at 780°C.The interface protection layer is necessary to achieve high-quality interface between the LPCVD-SiN_x gate dielectric and etched GaN.

Benefiting from the improved interface quality enabled by the PECVD-SiN_x protection layer, both the MIS-HEMT and MIS-FET deliver tiny hysteresis ΔV_{TH} < 0.1 V and small subthreshold swing SS ~ 97 mV/dec (Fig. 2) measured in a quasi-static setup featuring a 0.7 V/s V_{GS} ramping rate. The MIS-FETs suffer from a lower channel mobility (~160 cm^2/V·s) that leads to a relatively larger R_{ON} (~13 Ω·mm) because of the removal of the heterojunction channel, whereas the thin barrier layer remaining in MIS-HEMT could preserve higher carrier mobility in the gate-controlled channel that results in a lower R_{ON} (9.6 Ω·mm). Both MIS-HEMT and MIS-FET exhibit E-mode operation with a positive V_{TH} of 0.4 V and 2.37 V defined with I_{DS} = 10 μA/mm, respectively. However, the fabrication of partially recessed thin barrier MIS-HEMT faces challenge in V_{TH} uniformity control due to difficulties in precisely controlling the recess depth. Therefore, a much tighter V_{TH} distribution is observed in MIS-FETs with standard deviation of 0.31 V than 1.4 V in MIS-

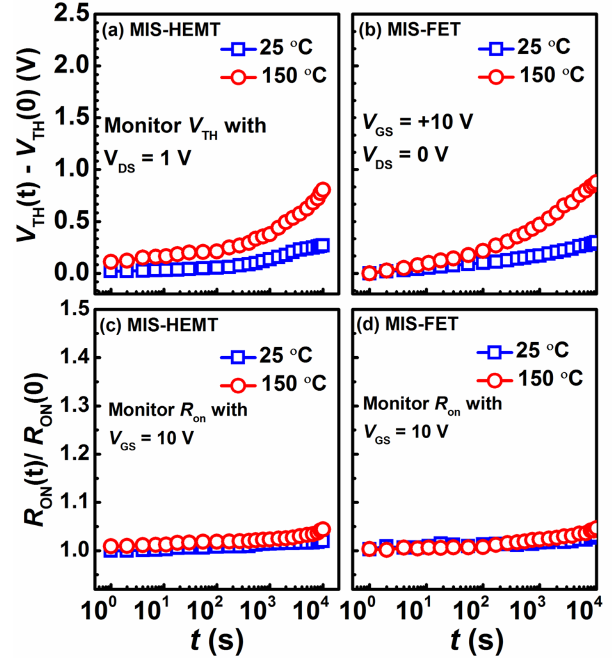

Fig. 4. Monitored V_{TH} and R_{ON} of (a)(c) MIS-HEMT and (b)(d) MIS-FET during the gate bias stress with V_{GS} = 10 V (PBTI)at both 25 °C and 150 °C (Device dimension: $L_{GS}/L_G/L_{GD}$ = 2/1.5/2 μm).

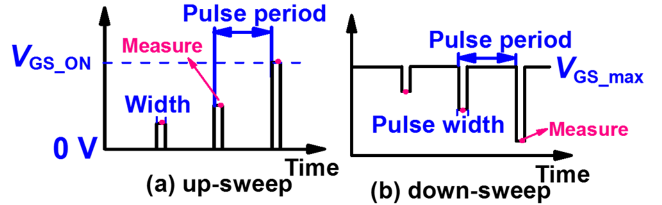

Fig. 5. Waveform of V_{GS} applied during pulsed I_D-V_{GS} measurement: (a) low-bias up-sweep and (b) high-bias down-sweep. pulse width and pulse period are 1 ms and 200 ms, respectively

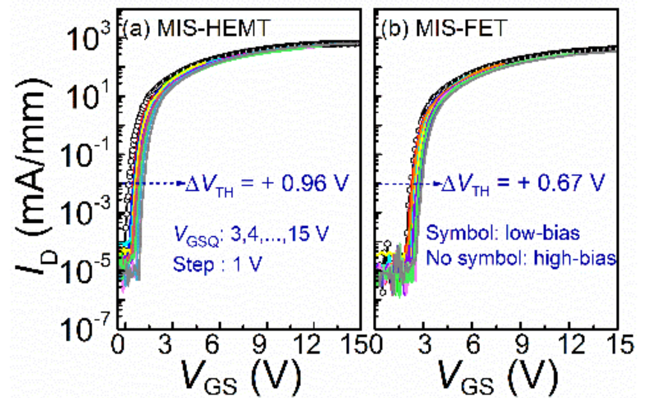

Fig. 6. Pulsed transfer characteristics of (a) MIS-HEMT and (b) MIS-FET with V_{GSQ} from 3 V to 15 V at RT.

HEMTs. In the temperature (T) - dependent transfer characteristics, the V_{TH} of MIS-FET exhibits significantly improved thermal stability compared to MIS-HEMTs, showing a smaller shift of -0.21 V in contrast with a -0.76 V in MIS-HEMT, from 25 °C to 200 °C.

Gate Bias Stress Measurement

PBTI stress was carried out on symmetric devices with a gate width W_G = 10 μm, a gate length L_G = 1.5 μm, and a gate/drain and gate/source spacing L_{GD} = L_{GS} = 2 μm. The devices were stressed for 10,000 s with drain bias V_{DS} = 0 V and gate bias V_{GS} = + 10 V, respectively. During the stress, the V_{TH} shift and R_{ON} induced by the PBTI stress were characterized by repeatedly interrupting the stress experiment for the execution of I_D-V_G and I_D-V_D measurement with V_{DS} = 1 V and V_{GS} = 10 V, respectively. To evaluate the effects of temperature, the PBTI stress was conducted at 25 °C and 150 °C. After the PBTI stress, the recovery was achieved by UV illumination for a few minutes. The transfer and output characteristics of both MIS-HEMTs and MIS-FETs can be fully recovered.

As demonstrated in Fig. 4, no significant variation in R_{ON} (< 20 %) was measured after stress even at high temperature of 150 °C for MIS-HEMT or MIS-FET. The V_{TH} exhibits a small shift of < 0.2 V at 25 °C for both devices and a slightly larger shift of + 0.9 V for MIS- FET and + 0.85 V for MIS-HEMT at 150C (?). Combined with the fully recovered characteristics after UV illumination, the V_{TH} and R_{ON} evolution during PBTI tests is very likely from the electron trapping process of the pre-existing traps at the dielectric/III-V interface and in the gate dielectric border near the interface[6]. When the channel is fully turned on, the gate voltage mainly drops across the dielectric. The same ranges of deep traps at the interface and/or the dielectric are filled with electrons coming from the channel under the same long-term positive gate bias, resulting in the identical PBTI behavior for MIS-HEMT and MIS-FET.

To reveal the impact of fast traps, a pulsed I_D-V_{GS} sweep measurement is conducted, which consists of a constant drain bias and a pulsed gate bias [7]. A set of pulsed measurements featuring low gate bias up-sweep and high gate bias down-sweep are performed to extract the hysteresis, as the waveform depicts in Fig. 5. The hysteresis between the low bias and high bias pulsed transfer characteristics is attributed to traps with a de-trapping time constant larger than the pulsed width. A critical V_{TH} hysteresis of +0.96 V in MIS-HEMT is observed as the bias voltage rises from 3 V to 15 V, while a reduced + 0.67 V hysteresis is obtained for the MIS-FET (Fig. 6). Under relatively large period (200 ms) positive gate bias, deep border traps in dielectric are filled. During the down-sweep, a thin barrier in the MIS-HEMT leads to deeper interface traps that cannot de-trap immediately within 1 ms pulse width, resulting in the more severe positive V_{TH} hysteresis in MIS-HEMT.

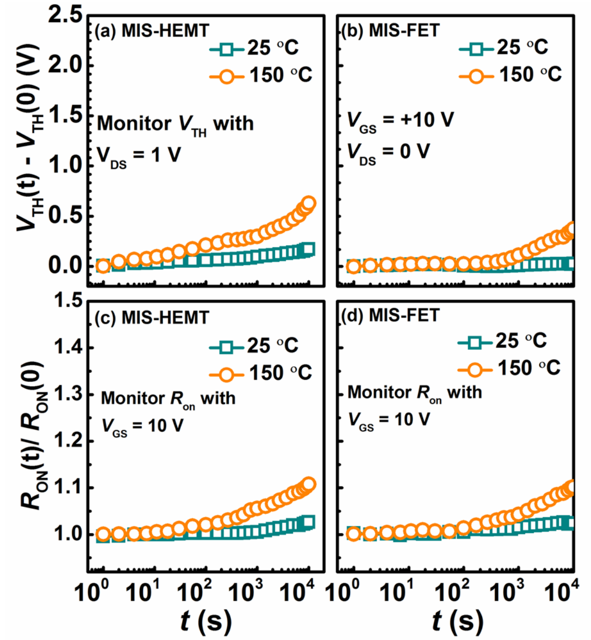

Fig. 7. Monitored V_{TH} and R_{ON} of (a)(c) MIS-HEMT and (b)(d) MIS-FET during gate bias stress with V_{GS} = -30 V (NBTI) at both 25 °C and 150°C.

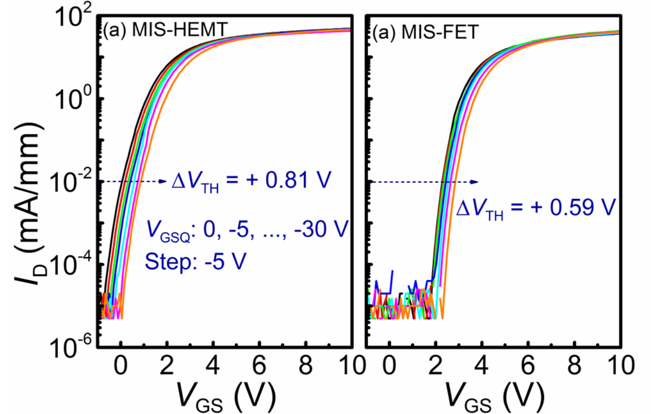

Fig. 8. Pulsed transfer characteristics of (a) MIS-HEMT and (b) MIS-FET with $V_{GSQ} < 0$ at 150 °C.

The MIS-HEMT and MIS-FET are also evaluated under NBTI stress measurements with the same setup as PBTI stress tests except that the gate stress bias was set to be – 30 V (Fig. 7). At 25°C, negligible V_{TH} instability and R_{ON} degradation over 10,000 s stress time are observed. Elevated temperature could cause more severe V_{TH} shift and R_{ON} degradation. MIS-FET exhibits moderately increased V_{TH} instability with only +0.46 V shift under -30 V gate bias in contrast with +0.67 V shift observed in MIS-HEMT. Dynamic transfer characteristics are measured with negative quiescent gate bias V_{GSQ} from 0 V to -30 V (Fig. 8). The pulse width and pulse period are 1 ms and 200 ms, respectively. The V_{TH} shifts positively (+0.81 V for MIS-HEMT and +0.59 V for MIS-

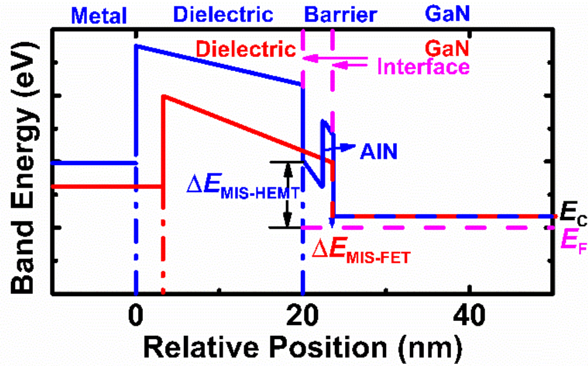

Fig. 9. Energy band diagram of MIS-HEMT (blue line) and MIS-FET (red line) at pinch-off state in the MIS-gate region.

FET) as V_{GSQ} decreases from 0 V to -30 V, consistent with the NBTI stress measurement. Both gate injection from the gate electrode to the gate dielectric or the dielectric/III-N interface [8] and Zener trapping [9] could result in positive V_{TH} shift. After the NBTI stress tests, the V_{TH} shifts could be fully eliminated with UV illumination, indicating that negligible new trap states are generated. The absence of negative V_{TH} shift under negative bias stress indicates the low-density of interface/border traps de-trapping under negative V_{GS}. The positive V_{TH} shift also suggests negligible hole trapping near the channel [10].

The difference of negative bias can be explained with band diagram as shown in Fig. 9. The fully recessed gate structure of the MIS-FET yields a smaller energy range of the interface trap levels above the Fermi level ((i.e. $\Delta E = E_C - E_F$) at pinch-off as a result of the barrier layer removal. Thus, more interface traps are buried below E_F and their charge states remain stable under negative gate bias, contributing to improved V_{TH} stability in MIS-FET. This could also explain the V_{TH} thermal instability in Fig. 3. The narrow ΔE in the MIS-FET indicates that less deep interface traps could participate in the thermally induced de-trapping, leading to enhanced thermal stability [11].

Conclusions

Device performance and stability of MIS-HEMTs and MIS-FETs have been systematically studied through static and pulsed measurements. Despite a slightly larger R_{ON}, the MIS-FET delivers superior V_{TH} uniformity and thermal stability. For the positive stress, similar PBTI behaviors and enhanced pulsed positive bias stability are obtained in MIS-FET compared with MIS-HEMT. For the negative stress, MIS-FET could also enable an improved stability in contrast with MIS-HEMT. Benefiting from a smaller range of deep interface traps responsible for electron trapping/de-trapping during bias stress and thermal measurements, MIS-FET yields the virtues of larger V_{TH}, process uniformity, and performance stability, making it a reliable power switch that exhibits enormous potential in the high-voltage power delivery systems.

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Acronym

MIS-FET: Metal-insulator-semiconductor Field Effect Transistor
MIS-HEMT: Metal-Insulator-Semiconductor High-Electron-Mobility Transistor
PECVD: Plasma Enhanced Chemical Vapor Deposition
LPCVD: Low Pressure Chemical Vapor Deposition
P(N)BTI: Positive (Negative) Bias Temperature Instability