Real Potential of GaN Electric Devices Coming From GaN on GaN

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Abstract

We present data showing greatly improved performance for AlGaN/GaN HEMTs, GaN PN diodes, and GaN Schottky diodes which were fabricated in GaN epi grown on lattice matched GaN substrates. These data are compared with devices having epi structure, layout, and processing, but where the GaN epi was grown lattice mismatched on one or more of the widely used silicon carbide (SiC), silicon (Si), or sapphire substrates. The GaN substrates used in this work were grown at SCIOCS using the Void Assisted Separation (VAS) method. The GaN epi grown on these lattice matched GaN substrates has three to five orders of magnitude lower dislocation density than the same epi structure grown on the above lattice mismatched substrate types. The very low dislocation density for GaN epi on GaN directly enables several impressive improvements in diode device performance parameters. These improvements for the GaN on GaN diodes include reduced reverse leakage currents, increased breakdown voltage, ideality closer to unity, and better controlled forward turn on voltages. We have observed that both forward and reverse diode I(V) characteristics in GaN on GaN diodes are very similar to the theoretically predicted I(V) predicted from GaN fundamental material parameters. This excellent text book diode behavior for GaN on GaN is in stark contrast to devices fabricated on lattice mismatched epi, whose performance is clearly limited by the high concentrations of point defects and the high dislocation density. The high defect and dislocation density is the inevitable result of lattice mismatched GaN epi growth. AlGaN/GaN HEMTs on native GaN substrates also showed greatly improved breakdown voltage (> 5kV) compared with nominally identical HEMTs fabricated in the same epi structure BUT grown on a lattice mismatched silicon (Si) substrates. Current collapse in the GaN on GaN HEMTs was also dramatically reduced. GaN substrate diameters of 100mm are now routine at SCIOCS, and 150mm GaN substrates have been demonstrated. Lattice matched GaN epi growth on GaN substrates clearly offers enormous performance advantages over ANY lattice mismatched substrate alternative.

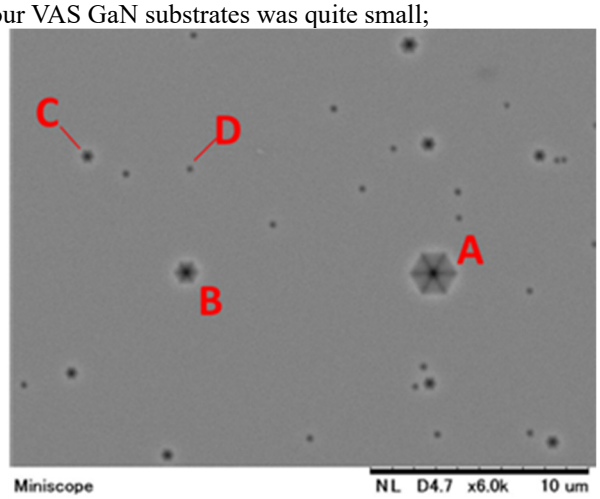
INTRODUCTION

Electronic devices based on GaN epitaxy exhibit several performance problems which are the direct result of defects caused by lattice mismatched epi growth. Both point defects and deep levels as well as extended defects like misfit dislocations are caused as the lattice of GaN accommodates the different lattice constant and crystal structure of the substrate beneath; this is an inevitable consequence of lattice mismatched epi growth. For GaN HEMTS the problems include current collapse, excess gate leakage, time domain transients, frequency domain dispersion, and memory effects which collide with complex modulation. For GaN Schottky and PN junction diodes, the mismatched growth causes idealities n>1, reduced forward turn-on voltages, excess reverse leakage currents, and unexpectedly low breakdown voltages compared with model predictions for GaN. The electron and hole ionization coefficients for GaN are known, and they are so small that the expected avalanche breakdown voltage for defect free GaN is should be very large, even for relatively thin GaN junctions (e.g., we expect BV ~ 150V for a 5000A thick GaN junction). However, these very large breakdown voltages and correspondingly low reverse leakage currents are essentially never realized in devices fabricated on GaN epi grown on lattice mismatched substrates. Instead, much larger reverse leakage currents, and much lower breakdown voltages are the norm. The types and concentrations of point and extended defects present in GaN epi depend strongly on what type of mismatched substrate is used (e.g., silicon, silicon carbide, or sapphire). The concentrations of certain types of GaN epi point defects also depend on the epi growth method (e.g., HVPE, MOCVD, or MBE) and on the growth conditions (e.g., MOCVD growth pressure) [1]. The concentration of GaN epi defects and dislocation densities are intricately dependent on epitaxial growth methods, growth conditions, and substrate type. Understanding these dependences comprises an active area of study in the field of GaN epi growth.

Recently, high-quality GaN substrates with very low dislocation density have become available from commercial suppliers, including from our company SCIOCS, where our GaN substrates are prepared by the Void Assisted Separation (VAS) method [2], which makes the dislocation distribution quite uniform both macroscopically and microscopically. This uniformity is quite important for the high device performance and is achieved only by VAS method in mass production. We present exciting electrical results which have been obtained on devices fabricated with GaN epi on VAS GaN substrates below, and show them to be greatly superior to devices made with conventional GaN epi which is usually grown on lattice mismatched substrates.

DISLOCATIONS AND VERTICAL DEVICES

It is well-known vassal plane dislocations in the SiC can be "killer defects" of SiC power devices [3]. This specific type of dislocation has also been shown to cause excess leakage currents and low breakdown voltages in GaN junction devices. We tried to locate and identify these killer defects using optical microscopy of samples which had been exposed to KOH etching. The KOH etch decorates individual dislocations which pierce the surface by forming a visible "etch pit" in the previously flat GaN epi surface, just as it does in GaAs. Fig.1 shows a typical image with the etch pits revealed by the KOH etch. The size of these pits varied for different dislocation types. We found the largest etch pits are formed on individual screw dislocations. These screw dislocations have been associated by others as the device performance degrading "killer defect" in GaN [4]. The smallest etch pits are the ones which form on pure edge dislocations. Etch pits of an intermediate size form on dislocations with mixed screw and edge character. The density of such presumed "killer defect" screw dislocations in our VAS GaN substrates was quite small;



	Size	dislocation
A	Big	Screw
B	Middle	Mixed
C	Middle	Mixed
D	small	Edge

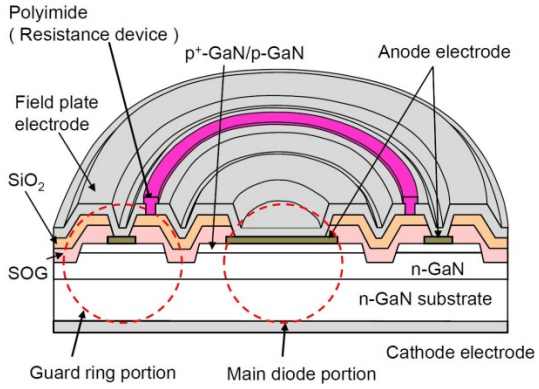
Dislocation Density of substrate
$\sim 3 \times 10^{6} cm^{-2}$
Density of screw dislocation
$5 \times 10^{3} cm^{-2}$

Fig.1 Optical microscope image of etch pits in Pits after KOH etching on VAS-GaN substrate

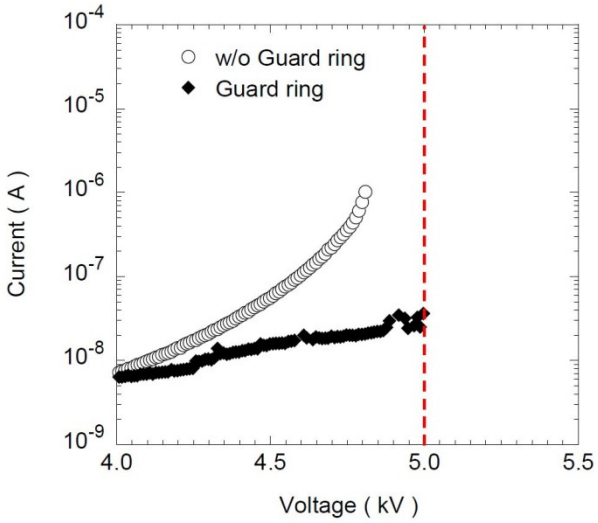
screw dislocations comprised only about 0.6% of the total dislocation density in our VAS GaN substrates. (This was shown by comparing the areal density of the large etch pits (screw dislocations) to the total Etch Pit Density from ALL dislocations (EPD in cm^{-2}).)

One can easily calculate the average number of screw dislocations within a given diode size (e.g., anode area) from the known areal dislocation density (defects/cm^2). These dislocations are quite uniformly distributed in our VAS-GaN material, so spatial distribution of these defects can be accurately modeled with a simple Poisson distribution. From the known dislocation densities of screw dislocations in the VAS GaN and the known diode junction areas, we were able make an important conclusion: we can conclude that screw dislocations (whose areal density is ONLY ~0.6% of the total EPD) must NOT be the defect which is contributing excess leakage and degraded breakdown voltage in our GaN on GaN diodes. This is because we observe very LOW leakage currents and EXCELLENT breakdown voltages, even in GaN on GaN devices which must have had at least one screw dislocation piercing the anode area. This is excellent news for device fabrication in GaN epi on GaN substrates. However, it does suggest another as yet unanswered question: exactly WHAT defect type(s) in the devices fabricated on GaN epi on lattice mismatched substrates are responsible for the excess reverse leakage and degraded breakdown voltage? This is not yet known. We believe the influence of dislocation should take account not only the dislocation type, but its localized density (when dislocations are condensed partially, that causes leakage in spite of the low average density) and interaction of point defects and impurity. These items must make the analysis quite complicated in case of high dislocated mismatch substrate case.

High purity GaN epi-layers for a PN diode structure were grown on low defect density VAS-GaN substrates (Fig 2) The diode layout and epi structure were carefully designed, and the fabrication process was optimized for low plasma damage, so as to control the electric field near the anode periphery, and to minimize damage induced periphery leakage current and resulting premature breakdown along the diode mesa sidewall. These diodes achieved a breakdown voltage of $\geqq$5kV, and diodes with a suitably designed guard ring, also had nearly 100X smaller reverse leakage current [5][6]. This performance may never be achieved on mismatch substrate.



(a) Device structure



(b) Breakdown Voltage

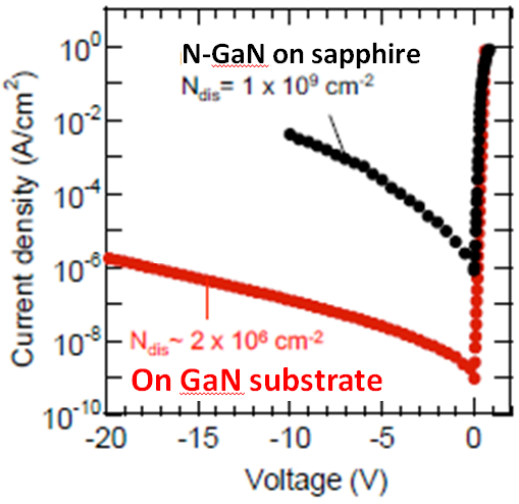
Fig.2 PN diode on VAS-GaN substrate. Copyright The Japan Society of Applied Physic (2018)[5]

In a separate study, GaN on GaN HBTs were compared with similar GaN on sapphire epi. As expected, the current gains hfe (and β) for the GaN on GaN HBT were over four times larger than the GaN on sapphire HBTs [7]. Presumably, point and/or extended defects from the lattice mismatched GaN on sapphire epi supported extra recombination in the emitter-base, which produced the observed four times larger base current and inferior current gain for lattice mismatched GaN on sapphire HBT.

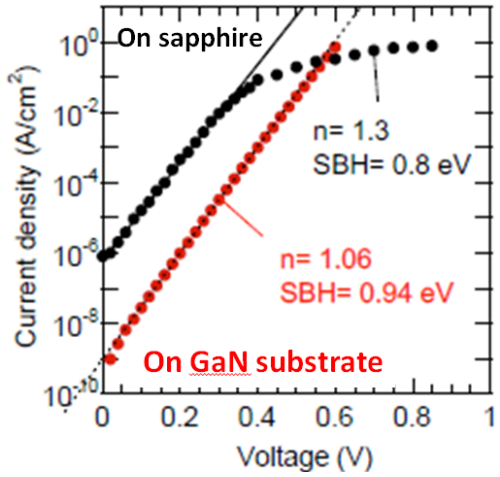
HORIZONTAL DEVICES

(1) Schottky performance

Schottky performance for GaN epi on GaN substrate was dramatically improved as compared with GaN epi on sapphire, as can be seen in Fig.3[8].

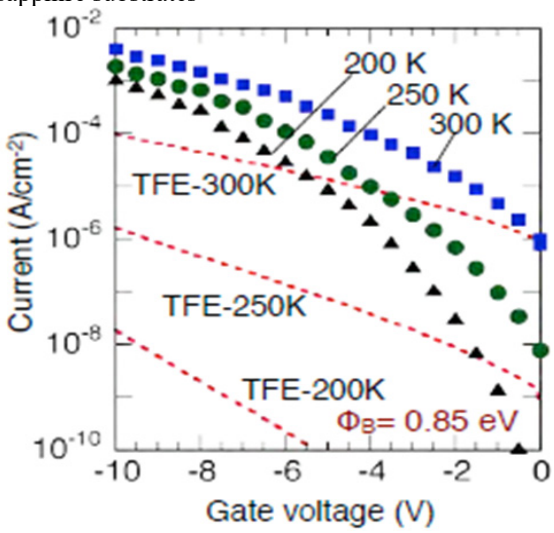


(a) Reverse bias

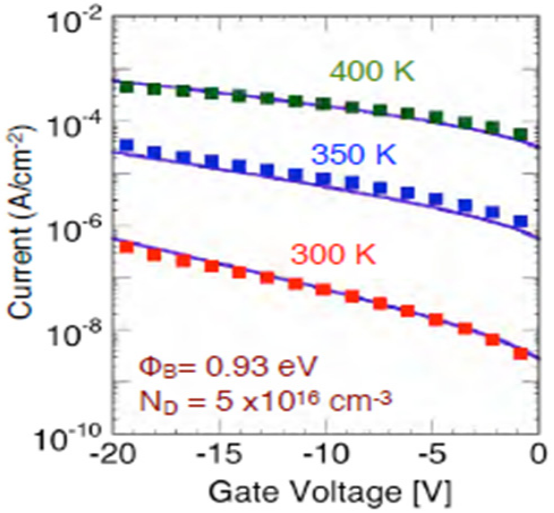


(b) Forward bias

Fig. 3 Schottky I(V) characteristic of n type GaN on GaN and sapphire substrates



(a) On Sapphire



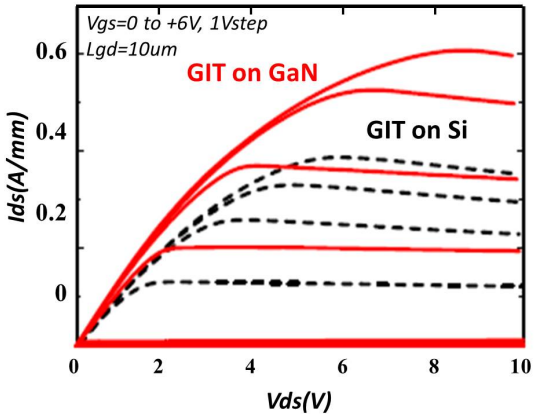
(b) On GaN

Fig. 4 Temperature dependence of reverse bias current

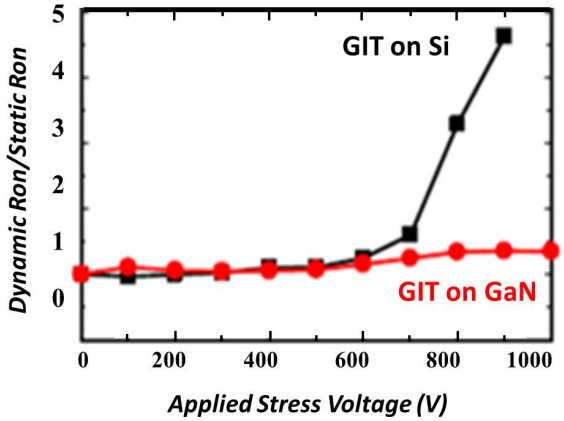
The reverse leakage current for the GaN on GaN Schottky diode is fully FOUR orders of magnitude smaller than that of the same device fabricated with GaN epi on sapphire (Fig 3(a)) The ideality factor for GaN on GaN diode is excellent (N= 1.03), but the GaN on sapphire has inferior ideality (N=1.30)(Fig 3(b)). Also, the detailed temperature dependence of the reverse I(V) for the GaN on GaN devices is in good agreement with predictions of the TFE model (Fig 4(b)). However, the GaN on sapphire diodes show a very different temperature dependent I(V) from the TFE mode (Fig. 4(a))l, which is undoubtedly the result of the participation of the defects formed from the lattice mismatched epi growth and making excess current. This confirms the idea that the devices fabricated on these low defect density lattice matched GaN on GaN wafers are exhibiting the FULL BENEFIT of extraordinarily low ionization coefficients and breakdown characteristics of intrinsic non-defective GaN.

(2) HEMTs

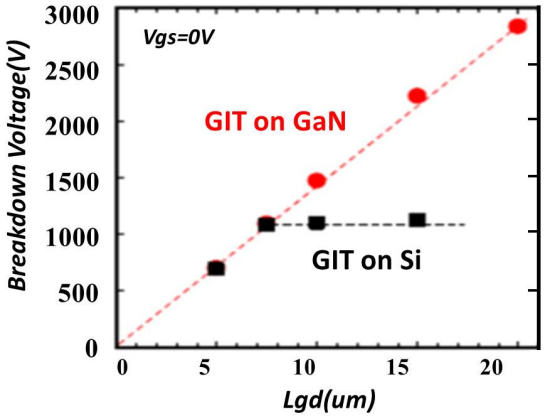
Panasonic has reported significantly improved GaN-HEMT device performance for devices fabricated on GaN epi on GaN substrates, as compared with similar devices fabricated of GaN epi on Silicon substrates [9].



(a) I-V characteristics



(b) Current collapse



(c) Breakdown voltage

Fig.5 Improvement of device performance by using GaN substrate in comparison with that on Si

These GaN on GaN HEMT devices showed higher saturated current Ids, and showed an absence of drain current collapse (see Figs 5 (a) and (b)). The GaN on GaN HEMTs also showed significantly higher breakdown voltages (>3kV), compared with the GaN on Si HEMTs which had breakdowns of only ~1kV (Fig.5(c)). The enhanced breakdown voltage in the GaN on GaN HEMT was achieved using a standard epi design and standard HEMT layout, as shown in Fig.6[10] No layout or epi design tricks were used to achieve this excellent breakdown voltage; it was the lattice matched GaN on GaN epi which provided this significant performance advantage.

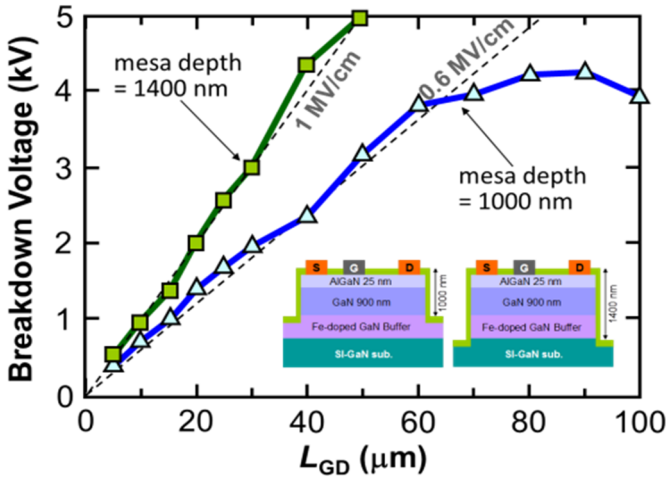


Fig.6 Extremely high breakdown voltage of HEMT on semi-insulating GaN substrate

Nonlinearity in RF performance was also significantly improved for the GaN on GaN HEMTs compared with HEMTs fabricated on lattice mismatched GaN epi .[11] This is to be expected because the reduced defect density in the lattice matched epi means there are fewer traps to

modulate the channel current Ids in the GaN on GaN HEMT. This reduces the frequency domain gain dispersion and the amplitude of 2nd and 3rd harmonics in the HEMT as compared with a lattice mismatched approach. Similarly, time domain drain transients in response to sudden change in gate bias should be significantly reduced for the GaN on GaN HEMT as compared with the lattice mismatched GaN HEMT because of the lower concentration of mismatch induce traps under the channel..

PREPARATION FOR MASS PRODUCTION

(1) Large size GaN substrate

SCIOCS has been producing VAS-GaN substrates in 2-inch (75mm) wafer diameter for some time. Recently, production of 100 mm diameter () VAS-GaN substrates has also become fairly routine, and we have now demonstrated 150 mm diameter (VAS) GaN wafers, using an improved growth method (see Fig. 7)[12]. We have even achieved a 7 inch (178mm) GaN wafer diameter (see Fig.8) by using a tiling method [13].

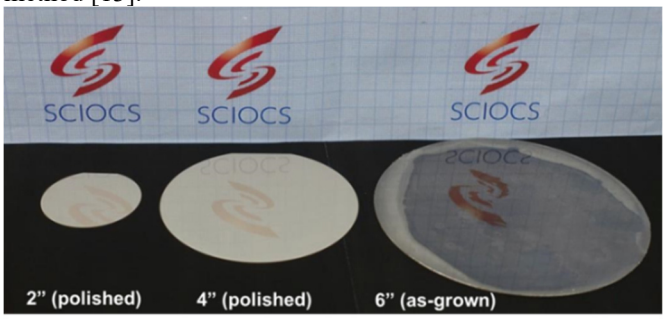


Fig.7 Large size VAS-GaN substrates. Copyright The Japan Society of Applied Physic (2018)[12]

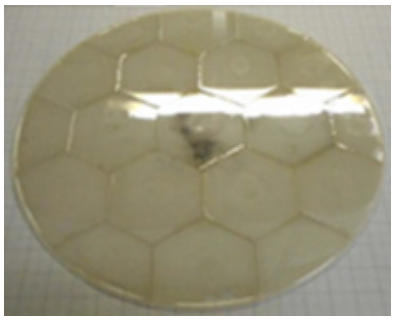
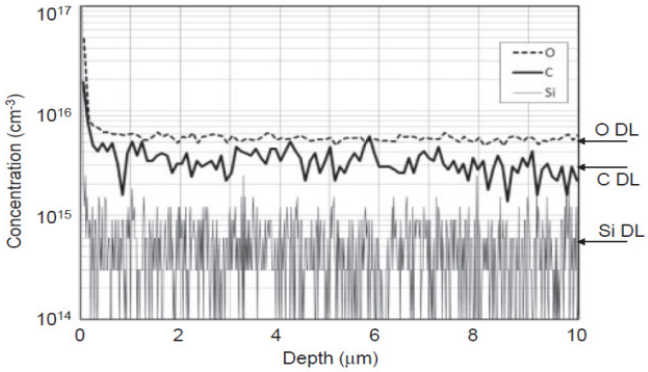


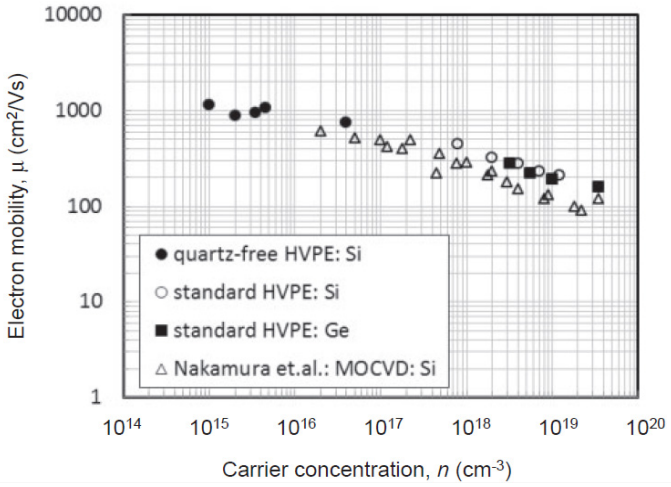
Fig.8 178 mm diameter GaN substrate using tiling method[13]

(2) High purity epi-growth by QF-HVPE

The drift layers of the vertical devices should be thicker (mostly more than 10um) and have very high purity (all the background must be lower than E15cm^{-3}) to achieve the high breakdown voltage. This layer is usually grown by MOCVD that takes long time, more than 10 hours for example, because the growth rate needs to be lower to decrease the carbon incorporation to achieve the high purity. HVPE has more than one order of magnitude faster growth rate and is carbon free, but has higher oxygen and silicon background coming from quartz parts of the reactor. The quartz free reactor was developed and very high purity GaN, with all the impurities under detection limit, was successfully obtained [14] as shown in figures 9, where Oxygen Carbon and Silicon concentration is under detection limit of SIMS and the mobility of n-GaN is very high, over 1000cm2/Vs. This growth technology will be able to provide low cost material.



(a) Impurity by SIMS measurement
(all atoms are under detection limit)



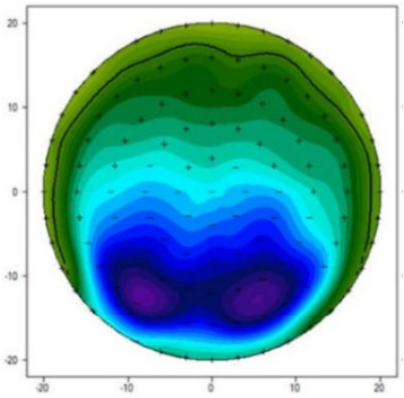
(b) Mobility of n-GaN

Fig.9 high purity GaN grown by QF-HVPE. Copyright The Japan Society of Applied Physic (2018)[14]

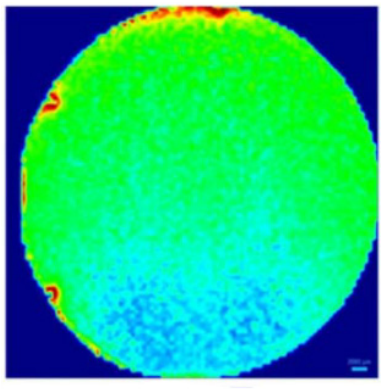
NON DESTRUCTIVE CHARACTERIZATION

Automated, non-destructive, accurate measurement and mapping of key properties of GaN epi wafers is essential for insuring high quality wafers for device manufacturing. Various characterization methods are applied to the lattice mismatched epi GaN on SiC, or GaN on Si, in order to measure GaN epi film thickness, defect density, etc, These techniques rely on the difference in refractive index (N,K) between the GaN epi and the underlying substrate. Such

techniques can also be used to measure AlGaN layer properties separately from the underlying GaN. However, for device structures using GaN on GaN, there is not any index difference between the GaN epi and the GaN substrate. Consequently, some of the traditional characterization tools applied to GaN on SiC or GaN on Si, are NOT useful for GaN on GaN. At SCIOCS, we have demonstrated new methods to fully characterize our GaN epi on GaN substrates. For example, we now extract GaN doping level and GaN epi thickness using a non-contact C(V) method[15]. We also characterize GaN and AlGaN/GaN surface morphology, and defect density using specially designed forms of -photoluminescence, FTIR [16] and surface light scattering [17][18]. The example of the mapping using the method is shown in Fig.10



(a) Carrier concentration



(b) PL of Carbon- related defect

Fig.10 Maps of n-GaN epi-layer by non-destructive method

(2018)[16][18]

CONCLUSION

We are now beginning to see real proof that GaN epi on GaN substrates provides significant improvements in device performance. The excellent reverse I(V) characteristics and high breakdown voltages observed in GaN on GaN devices are now comparable to theoretical limits imposed by fundamental GaN material parameters. This is excellent news; it means that GaN epi on GaN substrates is beginning to unlock the full potential of the GaN material system. In contrast, devices fabricated in lattice mismatched GaN epi (e.g., GaN on SiC, or GaN on Si, or GaN on sapphire) will forever be limited by the defects that are inevitably produced in lattice mismatched epi growth. These results all point to an exciting future for devices fabricated in GaN epi grown on lattice matched GaN substrates!

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ACRONYMS
GaN: Gallium Nitride
Si: Silicon
SiC: Silicon Carbide
HEMT: High Electron Mobility Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
HVPE: Hydride Vapor Phase Epitaxy
MBE: Molecular Beam Epitaxy
VAS: Void Assisted Separation
HBT: Heterojunction Bipolar Transistor
TFE: Thermionic Field Emission
FTIR: Fourier Transform Infrared Spectroscopy