High quality AlGaN/GaN HEMT for RF applications on cold-split thinned 4H-SiC substrates

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Abstract

AlGaN/GaN High Electron Mobility Transistors (HEMT) for RF application have been manufactured on SiC substrates thinned with a cold-split method, which allows a cost-effective wafering process. A properly tuned epitaxial growth process allowed depositing very uniform epitaxial layers, and the devices realized on those layers exhibited state of the art characteristics of HEMTs realized on standard substrates. This constitutes a successful first step for introducing an alternative wafering technology which significantly decreases material costs for SiC devices – without device performance degradation. It also proves the robustness of the epitaxial process and its adaptability to thinner SiC substrates.

INTRODUCTION

High frequency power electronics based on AlGaN/GaN HEMTs have been developing very fast in the last years. These devices target fast and efficient transmissions of high volume of data, where low power losses are important [1]. The fields of application range from high-speed mobile communication to technology for space applications. These devices are manufactured on semi-insulating 4H-Silicon Carbide (S.I. 4H-SiC) substrates, because they offer excellent thermal conductance, which is crucial to dissipate the heat generated during operation [2]. The realization of these devices is costly, due to high level of technology and materials required, with the substrate having the largest impact on cost. Although the value of these transistors is really high, outperforming what is achieved with other compound semiconductors [3], the final cost of a device may be seen as a limitation in their widespread use.

Several techniques have been developed in the last years in order to remove the epitaxial layers stack from the substrate, which can then be either recycled (as in the case of GaN substrates) or completely eliminated (as done for silicon or sapphire). These techniques consist in the lift-off of the GaN epilayers through laser lift-off [4], etching of thin intermediate layers such as InGaN [5], lift-off through the detachment of weakly bonded h-BN layers [6], or with chemical etching of the substrate (e.g. silicon) [7]. Although all of the abovementioned techniques could be applied also in the case of RF AlGaN HEMT structures employed in this study, they would all lack the unique advantages given by the semi-insulating 4H-SiC substrates, with their hardness, chemical inertness, high resistivity, and high thermal conductance. Therefore it is reasonable to not remove the substrate, rather to keep it but with the minimal thickness required and possibly with a lower cost.

A typical AlGaN/GaN HEMT is manufactured on a 500 µm thick 4" S.I. 4H-SiC substrate. Once the epitaxial layers are deposited and the whole device structure is realized, the substrate is thinned down to approximatively 100 µm. That means that 400µm of valuable SiC material is lost during the back side grinding process. In this study we would like to demonstrate that by replacing back side grinding with a laser assisted splitting technology, these 400µm of unwanted SiC material can be utilized for a second device run.

Siltectra GmbH developed the Cold Split process [8], which allows slicing directly 50-500 µm thick SiC substrates

Fig. 1: Full view of the split off 100 µm thin 4" wafer.

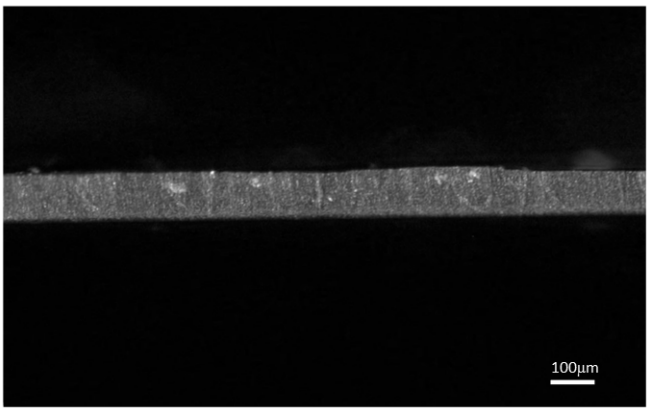

Fig. 2: Side view of the split off thin wafer. Polished side down, split side up. The average thickness is 95 µm.

from a boule or a wafer with a total loss after CMP of less than 100 µm. In this study, an initially 500µm thick standard semi-insulating SiC wafer was thinned using Cold Split. In Figure 1 the resulting 100µm thick split off wafer can be seen, as well as a cross section image in figure 2 (please note that the Si-side was split off). The remaining part of the wafer became the starting point that can be used as another substrate for device manufacturing in this study. The wafer was ground and CMP polished using standard industry processes. After that, the wafer had a thickness of 350µm.

In this way the cost of the substrate can be dramatically reduced, because the formerly ground-down SiC material during backside thinning is now used as substrate for a full second device run. This potentially doubles the device output of a single SiC wafer and would almost halve the SiC material cost per device.

In this work we demonstrate the feasibility of every step of a transistor production on the thinner initial SiC wafer derived by the Cold Split process. We will show that only minor adaptions are required to achieve state-of-the-art

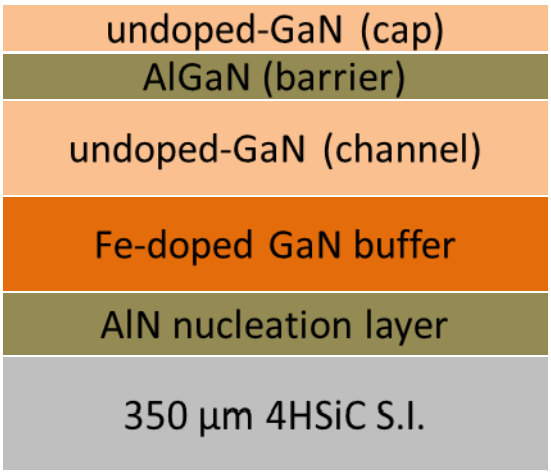

Fig. 3: Epitaxial layers sequence used for all the growth experiments for a AlGaN/GaN HEMT structure

characteristics of the final devices. This validates the use of Cold Split instead of traditional back side grinding to dramatically lower the overall costs of AlGaN/GaN HEMT on SiC and boost their utilization in the RF device market.

EXPERIMENTS AND RESULTS

Commercial 4" S.I. 4H-SiC substrates, 500 µm thick, from two different vendors (A and B), were thinned down to 350 µm either with the cold-split process or with mechanical grinding. The thinned substrates were then polished to an epi-ready status through chemical-mechanical polishing (CMP).

The substrates were analyzed with different characterization techniques. Optical microscopy with Nomarski differential-interference contrast (NDIC) and atomic force microscopy in tapping mode (AFM) showed that the CMP substrate was ready for the epitaxial growth. Defect density estimated through optical inspection did not show any deviation from standard substrates, if not for a higher density of micropipes in the substrate from vendor A. The bow and warpage of the wafers was within 10 µm, independently from the thinning procedure, and comparable with a standard 500 µm-thick substrate.

The epitaxial growth was performed in a multi-wafer MOCVD reactor. The typical stack of layers for the targeted transistors, consist of a thin AlN nucleation layer for lattice matching of the GaN layers on the SiC substrate, followed by a highly resistive buffer of iron doped GaN [9], then an undoped GaN layer serving as channel, and finally a thin barrier layer of AlGaN, protected by a thin GaN cap (Figure 3). The use of thin substrates for a hetero-epitaxial growth process may be a challenge, due to the different strain for the different crystalline materials grown atop each other, which generate compressive or tensile strain. Indeed the wafer tends to bow during the epitaxial growth; a large bow is

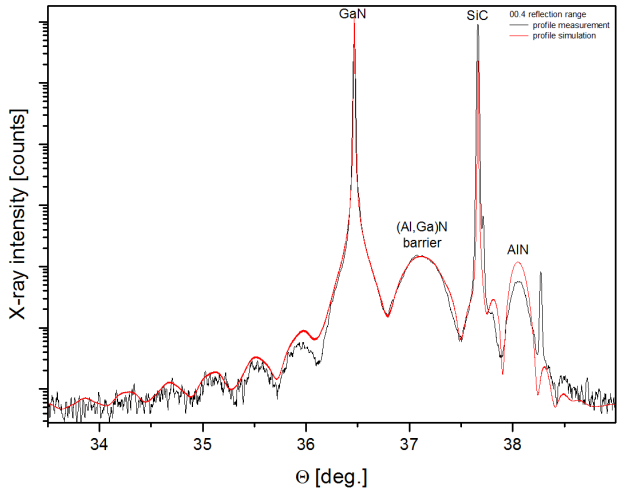

Fig. 4: 00.4 Θ/2 Θ-scans on an HEMT structure deposited on cold-split thinned substrate

detrimental both for the epitaxial growth and for the device processing. Usually thick substrates offer a mechanically stable base to grow a stack of different epitaxial layers, keeping the final bow of the whole wafer low (below 30µm). In the epitaxial growth process, we have tuned the thickness of the AlN nucleation layer to influence the wafer bow during growth. In this way, not only devices can be manufactured without issues, but at the same time the temperature uniformity of each wafer during the epitaxial growth could be kept low. In fact, temperature differences above 2-3 K across the whole wafer can impact negatively both the thickness of each epitaxial layer, and the composition of the alloys, such as the AlGaN barrier. For this purpose, not only it was beneficial to keep a low wafer bow during the growth, but also the adaptation of convex-shaped wafer holders in the MOCVD reactor, assured temperature variations below 2K within wafer.

These optimizations led to very uniform epitaxial layers, as indicated by HRXRD measurements of the thickness and composition of the AlGaN barrier and GaN cap (Figure 4), whereas the center-edge difference was: 0.2 nm in thickness, below 1% in the Al-content. Slight differences were found between the wafers supplied by the two vendors, with the wafers from vendor A having a thicker barrier but lower Al content. Measurements of the sheet resistance also proved the layer uniformity with standard deviation below 1.5% on an average value of 410 Ohm/sq for vendor B (Figure 5). The wafers from vendor A resulted in a higher average sheet resistance of 427 Ohm/sq and a standard deviation of 2 to 3%. The analysis with optical microscopy did not show any irregularities in the typical surface morphology, and showed a very low defect density, typical for this epitaxial structure. Even the surface roughness measured with AFM resulted in roughness value below 0.3 nm on a 10x10 µm^2 scale, which

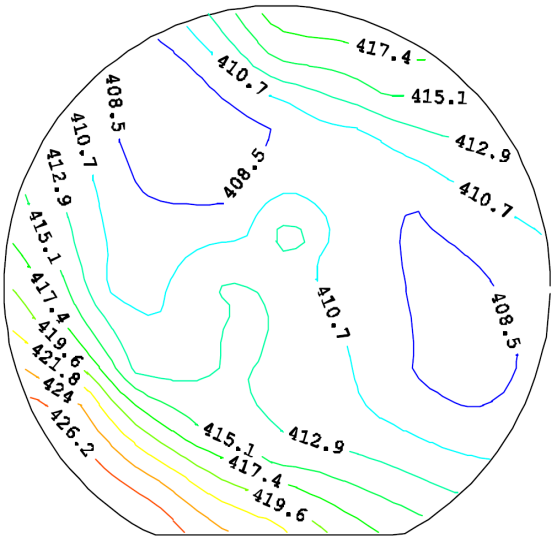

Fig. 5: Sheet resistance map of a HEMT structure, deposited on a cold-split thinned substrate. Average value of 413 Ohm/sq, with a standard deviation of 1.2%.

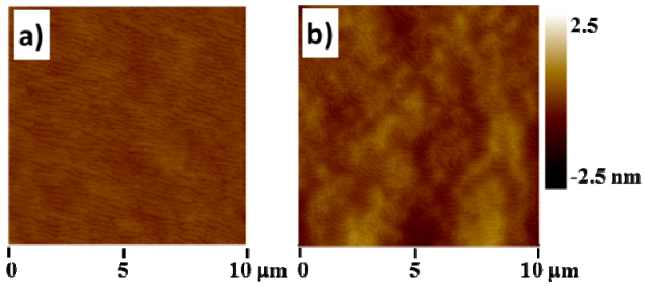

Fig. 6:10x10 µm^2 scans by AFM of a thinned substrate: a) before the epitaxial growth (RMS = 0.12 nm); b) after the epitaxial growth (RMS = 0.27 nm).

is also typical (Figure 6). Last but not least, the bow and warpage of the 2 µm-thick epi layer was below 30 µm (Figure 7), which allowed the wafers to be processed at a device level.

Device processing is carried out using both electron-beam and stepper lithography. It involves isolation by implantation and alloyed Ti/Al-based ohmic contacts optimized for low contact resistance (below 0.25 Ohm×mm) and smooth edges for improved marker recognition. The gate is defined by electron beam lithography. As a key element for high speed operation the gate head is designed to achieve low parasitic capacitances. SiN passivation

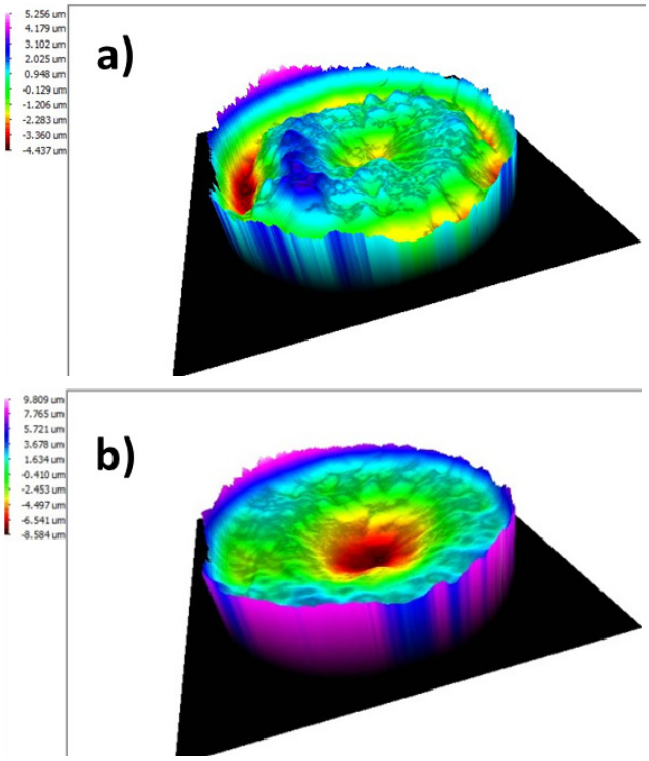

Fig. 7: Bow and Warp of a thinned substrate: a) before the epitaxial growth (bow = -2 µm, warp = 10 µm); b) after the epitaxial growth (bow = -10 µm, warp = 18 µm).

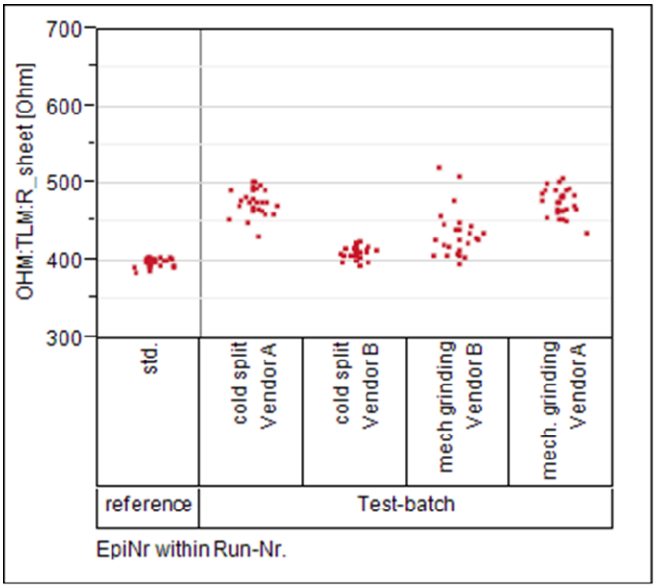

Fig. 8: Sheet resistance on wafer for the same HEMT structure on different substrates: std. = standard 500 µm; vendor A and B, thinned to 350 µm either by cold-split or mechanical grinding.

optimized for low current dispersion and thermal stability is deposited. Furthermore, fabrication of integrated circuits comprises processing of NiCr thin film resistors, MIM capacitors, interconnect metals, electroplated Au airbridges, and inductors.

The GaN10 technology, with submicron source-gate and gate-drain spacings, exhibits good uniformity across individual wafers, as well as high repeatability between several wafers in a single batch or even between different processing batches. The achieved saturation currents were estimated to a value of 1.5 A/mm. The extracted maximum DC-gm on PCM-transistors were beyond 500mS/mm.

The overall results exhibited that no differences in the electrical characteristics of the transistors exist between those made on a standard 500 µm-thick substrate and those made on the substrates thinned, either with the cold-split process at Siltectra, or by mechanical grinding. It is noteworthy saying that the wafers thinned with the cold-split process showed a lower standard deviation for several electrical characteristics (Figure 8).

Conclusions

4H-SiC S.I. substrates thinned with a cold-split process have been used to deposit a AlGaN/GaN HEMT structure, and devices have been fabricated. The quality of the epitaxial layer and the electrical characteristics are perfectly comparable with similar layers deposited on standard thicker substrates. This proves that thinner SiC substrates can be used successfully with minor tuning of the epitaxial growth process, without any deterioration of the transistors.

Thanks to the high cost effectiveness of substrates yielded with the cold-split process, and to the maintained characteristics of transistors deposited on these substrates, AlGaN/GaN HEMT on SiC can win a substantial gain in the market of RF devices.

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Acronyms

HEMT: High Electron Mobility Transistor
S.I.: Semi-insulating
HRXRD: High resolution X-ray diffraction
MIM: Metal-Insulator-Metal
MOCVD: Metallorganic Chemical Vapor Deposition