

The Reliability of Compound Semiconductors, Proving It's Good Enough

William J Roesch

Qorvo, 2300 N.E. Brookwood Parkway, Hillsboro, Oregon 97124-5300

Phone: (503) 615-9292

EMAIL: bill.roesch@Qorvo.com

ABSTRACT — Compound semiconductor circuits are flourishing in high volume production which has been expected and predicted for several years. As these GaN and GaAs circuits become more widely considered for use in applications of various electronic systems, instruments, and devices, questions regarding reliability arise.

Key Words — reliability, failure, mechanisms, building-in, device physics, continuous improvement

I. INTRODUCTION

Compound Semiconductors (CS) such as Gallium Nitride and Gallium Arsenide have long been labeled as “the semiconductor technology of the future.” However, once the cell phone became the largest consumer application known to mankind, perhaps the future has finally arrived for these technologies. Use of compound semiconductors in cell phones is enabling and ubiquitous. The growth and size of mobile devices has been measured as the largest worldwide consumer of electronics for more than five years.^[1]

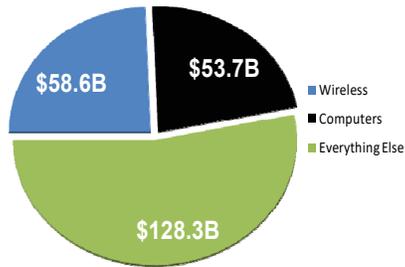


Fig. 1. Spending on microchips used in smartphones, tablets and related wireless devices for 2011.

The explosion of GaAs volume in applications in consumer wireless devices has brought transitions in manufacturability, cost, quality, and reliability that wouldn't have ever been expected from the previously tiny compound semiconductor niche. The advent of “smart” phones and tablets have further solidified the presence of GaAs devices in places where linearity and data bandwidth requirements demand the unique performance aspects of compound semiconductors. 25 years ago, nobody predicted that >10 Billions of compound circuits would ever be utilized annually.

But what about GaN? What's holding back the other compounds such as GaN and InP? What reliability aspects are needed for high performance and wide bandgap materials to reach their potential?

II. HISTORY OF COMPOUND SEMICONDUCTOR RELIABILITY

The basics of reliability in semiconductors are timeless and technology agnostic. Regardless of materials, applications, or performance, there are five distinct stages of reliability development in Table 1.^[2]

TABLE 1. STAGES OF RELIABILITY

Era	Reliability Steps	Qualification Styles
1	Materials	Process Integration Compatibility
2	Problems Failure Mechanisms	One dimensional stress to failure
3	Physics Stress Models	Success testing
4	Engineering Built-in Reliability	Capability edges & simultaneous stressing
5	Defects Capability & SPC	Continuous Improvement

Whether it is a semiconductor or an automobile, the development of reliability takes some time and some period of acceptance. Because of the experience elements of “building-in” reliability and continuous improvement are driven by volume, it's often a sticking point for new technologies to break through these experience barriers. Early adopters are expected to experience reliability challenges that are anticipated to be removed by maturity of the full experience of the five stages of reliability. An example of risk avoidance is shown by reluctance of folks to buy a new model automobile during its introductory year.

When one examines the beginning of integrated solid state electronics, the advent of Moore's Law in 1965 is unavoidable.^[3] However, those of us in the compounds may also remember that 1965 was the same year that Edward Johnson's less famous “Figure of

Merit” was launched in his company’s *RCA Review* with this title: “Physical Limitations on Frequency and Power Parameters of Transistors.” Mr. Johnson’s Figure of Merit supposed “that an ultimate limit exists in the trade-off between the volt-ampere, amplification, and frequency capabilities of a transistor.”^[4] Both Moore’s and Johnson’s theories were aimed at predicting trends of future semiconductor developments. However, neither the mainstream silicon, nor the compound semiconductor folks typically remember these two quotes from Gordon Moore’s paper...

“Reliability Counts.”

“Silicon is likely to remain the basic material, although others will be of use in specific applications. For example, gallium arsenide will be important in integrated microwave functions.”

Gordon E. Moore,^[3] 1965

For mainstream silicon device technologies, Moore’s Law has provided the miniaturization drumbeat for each stage of reliability. Without the afore-mentioned volume, GaAs technology struggled to get beyond the initial three stages in Table 1, and compound semiconductor users remained skeptical through the 1980s and 1990s.

In spite of the early brand of GaAs as “the technology of the future,” hard work through all stages of reliability resulted in devices with acceptable (if not exceptional) levels of reliability. The body of results for Compound Semiconductors has been summarized several times during the maturation phase of technology development shown in Figure 2.

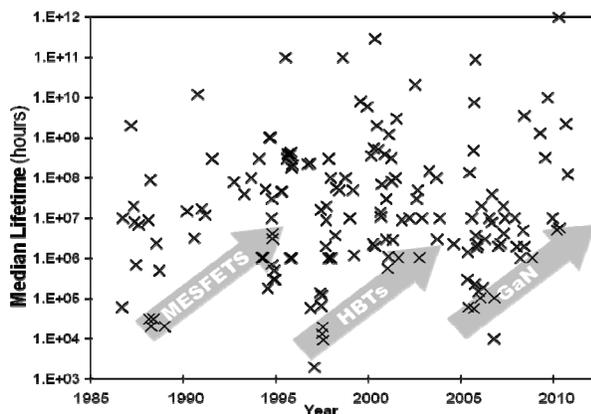


Fig. 2. Predicted lifetimes reported for compound semiconductors.[5]

On the other hand, the relentless pursuit of Moore’s Law has made reliability a new and daunting challenge

for the latest materials needed to continuously shrink the silicon CMOS technology for over five decades. Although comfortably long lifetimes have been enjoyed by the mainstream technology, recent accomplishments and the associated new materials have chipped away at the longevity of silicon lifetimes enjoyed in previous generations. Without question, Moore’s law has driven reliability of mainstream silicon lifetimes back within sight of high reliability applications...

“Adherence to Moore’s Law is creating a reliability gap”

Craig Hillman,^[6] 2009

This gave the compounds an opportunity to win favor.

III. SEMICONDUCTOR RELIABILITY DEFINED

There are two key parts to a definition of reliability. First, is a measure of “goodness” which is most easily described by using existing definitions of quality. Examples of these measures might be: conformance to standards, meeting expectations, or compliance to certain specifications. Typically, measures of “goodness” are replaced by definitions of what is not good enough. For example, most semiconductor reliability engineers speak in terms of failure rates instead of success probabilities. As the “rate” mentioned above implies, the second major part of a reliability definition involves time. Expected periods of “goodness” may range from several seconds for a guidance system in a missile, to decades for a communications system in an airliner or satellite. Other significant parts of a definition might include environmental conditions and duty cycles. A basic definition of reliability is quality for a length of time with an included environmental stress.

The measurement of reliability for semiconductors generally involves failure rates. Traditionally, several classifications of failure types have resulted from the failure experience of large systems during their use. This experience is commonly translated to the “bathtub curve”. Whether measuring computers, automobiles, or even human lifetimes; early and wearout failure types are generally expected.

Early or infant failures refer to systems which fail long before normal wearout would be expected. Early failures are attributed to devices or assemblies with manufacturing defects or problems. Consumers have been historically protected from these early failures by a warranty. For the first five decades of the electronic age, early failures in silicon technologies have been screened by a practice known as “burn-in,” where devices or systems are turned-on for a short period of

time before being delivered to customers. Occurrences of early failures decrease significantly as devices age, so burn-in has been effective in preventing warranty failures. Over the years, burn-in was optimized by elevating the temperature. This thermal acceleration caused early failures to occur faster, and allowed manufacturers to ship products sooner.

From the beginning, compound semiconductor manufacturers discovered that eliminating manufacturing flaws during fabrication is a more cost-effective method of reducing early failures than screening individual devices with burn-in. Admittedly, some naivety and lack of volume helped make this approach successful.

The wearout period is characterized by increasing failure rates. Gradual degradation in device parameters is typical for GaAs devices when subjected to extremely accelerated life-test conditions. Occasionally, this degradation leads to functional failure, but in all cases, catastrophic failure mechanisms are rare except when devices are overstressed, either by application or design.

For the system designer, early and wearout failure risks must be considered for the selection of each component. The infant and wearout failure periods are dependent on device processing, testing and screening. The IC designer can favorably impact these areas only by following design rules and guidelines. The wearout failure period has been the IC designer's main concern. Design errors will often result in excessive early and random failures, however.

The strategy to accomplish and verify the reliability goals involves testing the individual building blocks of ICs. These building blocks are labeled "elements," and they consist of each metallization interconnect type, resistors, capacitors, contacts, and transistors. Element testing is optimal for a number of different reasons. It is essential to isolate and assess all the various failure mechanisms possible for an IC. Element testing is especially useful to the circuit designer because the data can be used to model the reliability performance of circuits based upon physical sizes and operating conditions of each portion of the design. Element tests have been used to verify, and in some cases, modify design rules. The strategy involves the following steps:

Steps to improve reliability:^[7]

- i. Conduct fundamental reliability studies to identify and measure wearout mechanisms for each IC process.
- ii. Calculate failure rates of each IC element. Continue process improvements until each element's reliability exceeds goals.

- iii. Model how temperature, voltage, current density, and other operational conditions or environments affect the time to failure of each element.
- iv. Select the maximum ratings for each element, consistent with the reliability goals.
- v. Publish the maximum ratings and guidelines.
- vi. Monitor reliability in actual use [natural conditions] and compare results with reliability expectations based on [accelerated conditions] element and IC predictions.^[8]
- vii. Re-evaluate elements as necessary and lifetest circuits (to failure) as they become available.

As part of the reliability investigation of GaAs technology many millions of devices have been stressed and evaluated.^[5] The data demonstrates that the GaAs process is capable of producing reliable products. Subsequent data collected on products and systems has shown that the IC data correlates well to results predicted by element testing. Stressing devices to wearout and the detectability of defects are essential in measuring device reliability.

IV. KEY ASPECTS INFLUENCING RELIABILITY

There are three areas of consideration when considering reliability of semiconductors. The first aspect has to do with the semiconductor fabrication process, the second aspect has to do with the design of the product, and the third aspect is the application.

While these aspects are universal for semiconductors. The influences are considerably different and those contrasts are the subject of the remainder of this work.

Fabrication, application, and design are three major factors controlling the ultimate reliability of integrated circuits. Manufacturing processes must be capable of demonstrating inherent reliability regardless of device function or complexity. This aspect is handled by maintaining a controlled process which has been developed with reliability as an integral goal. Proving the inherent reliability of gallium arsenide devices has been the main objective of GaAs reliability programs for more than 25 years.

Another key aspect of circuit reliability is the application or insertion of devices, with correct handling and assembly procedures, into an adequate environment for their intended use. This is the area that is least controllable by the foundry, and is also usually somewhat removed from the design. Unfortunately, because of this detachment, many of the early users of gallium arsenide had difficulties with application problems such as environmental overstress, electrostatic discharge, improper heatsinking, and poor impedance matching.

Lastly, some aspects of reliability are controlled by the design of the circuits, whereas even the best processing can yield devices which fail prematurely in their intended applications. These “design-controlled” aspects are the major emphasis of the following discussion on GaAs reliability.

V. EXAMPLE: BUILDING-IN RELIABILITY & DEFECT REDUCTION BY DESIGN

The fourth and fifth stages of reliability are critically important in reducing reliability risks for customers. Building-in reliability is achieved by improving all aspects of anticipation and predicting reliability issues, preventing problems proactively in the manufacturing process, and mastering methods of detection, measurement, and characterization to protect customers.

Compound semiconductor manufacturing processes will typically utilize metallization patterning techniques called “lift-off.” In addition to being a unique construction procedure, lift-off is also a challenging photolithographic method. The quality of lift-off is commonly evaluated subjectively by inspection: either optically or by use of a scanning electron microscope. Elemental study offers an alternate method of measuring lift-off quality by using specially designed structures that can be evaluated electrically. These measurements are not only objective and quantitative, but they can be highly automated.

As a result of using special elemental test structures and electrical measurement techniques, manufacturing technology can be translated to design and layout aspects:

- A. Structures capable of detecting lift-off anomalies by simple electrical measurements have been developed.
- B. The dimension of physical space between metal electrodes has been demonstrated as an amplifier of defect detection.
- C. Voltage can be combined with physical amplification to further accelerate defect measurements as alternatives to increasing areas and peripheries of monitor structures.
- D. A similarity between metal shorting defects caused by lift-off and extrinsic capacitor defects is noted.
- E. Voltage and time were found to be roughly interchangeable in their ability to accelerate reliability failures.

Figure 3 shows how the defectivity is impacted by spacing on a volt*centimeter basis. Testing elements to

failure is a good substitute for high volume in emerging technologies.

VI. CONCLUSION

Regardless of the manner of testing, proving, or building-in reliability, the only proof of delivering to the expectation comes in the actual application and use of any particular technology. The immense consumer electronics demand for mobile devices is the true testament that compound semiconductors have become some of the enabling technologies of today. The harder question to answer is: “What will prevent GaAs and GaN from becoming the technologies of the past?”

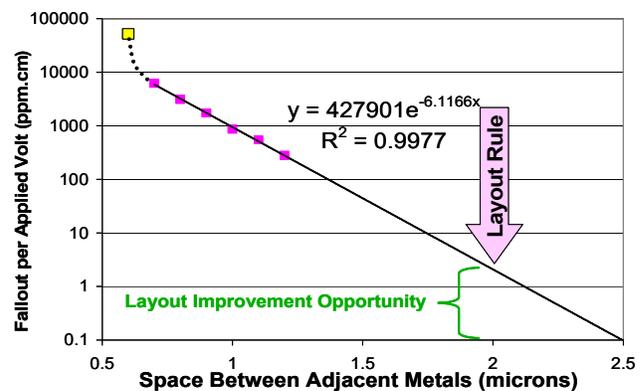


Figure 3. Predicted defectivity in Parts Per Million per centimeter per volt.^[7]

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REFERENCES

- [1] M. Hamblen, “Spending on chips for mobile devices outpaced computers in ‘11,” *Computerworld*, February 1, 2012.
- [2] H. Stork, “Reliability Challenges for Sub-100nm System on Chip Technologies,” Keynote Address, International Reliability Physics Symposium (IRPS), 2004.
- [3] G. Moore, “Cramming more components onto integrated circuits” *Electronics Magazine*, Volume 38, Number 8, April 19, 1965.
- [4] Edward O. Johnson, “Physical Limitations on Frequency and Power Parameters of Transistors,” *RCA Review*, vol. 26, 1965, pp. 163-177.
- [5] W. Roesch, “The ROCS Workshop and 25 Years of Compound Semiconductor Reliability,” *Microelectronics Reliability*, pp. 188-194, Volume 51, Issue 2, February 2011.
- [6] C. Hillman, “Does Silicon Wearout: An OEM’s Perspective,” *IEEE SCV Reliability*, October 28, 2009 Cupertino, CA
- [7] W. Roesch and D. Hamada, “Measuring Lift-off Quality and Reliability with Special Test Structures,” International Conference on Compound

Semiconductor Manufacturing Technology, pp. 199-202, April 14-17, 2008,
Wheeling, Illinois, USA. [He Bong Kim Best Paper Prize Winner]

[8] W. Roesch and S. Brockett "Natural Failure Mechanisms: Analysis of Actual
Field Returns," pp.55-71, Reliability Of Compound Semiconductors
Workshop. November 12, 2006, San Antonio, Texas.