Fabrication of 4-inch GaN/Diamond HEMT in a Compound Semiconductor Foundry

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Abstract

This work demonstrated a successful fabrication of 4 inch GaN/Dianond HEMT wafers in a 4-inch compound semiconductor foundry. The challenges and solutions in wafer processing were discussed. DC/RF device parameters were measured on-wafer and compared with GaN/SiC counterparts. Power density of 4W/mm at Vds=28V and 7.8W/mm at Vds=50V and PAE of 58% were obtained from wafer level 2GHz CW power measurements.

INTRODUCTION

GaN-based HEMT technology for RF applications has been maturing and is widely employed in various commercial and military applications. 50V CW applications with >10W/mm saturated output power density are fairly common. A >100V S-band 200W discrete transistor has been demonstrated recently [1]. With the increasing operation voltage and power, heat dissipation becomes the key technological barrier hindering further progress of GaN-based RF transistors.

On the other front, advances in CVD diamond technology make synthetic diamond an ideal substrate for GaN devices due to its excellent thermal conductivity (up to 20 W/cmK). In the past few years, with the improvement in microwave CVD diamond synthesis process, researchers at Raytheon and TriQuint successfully demonstrated enhanced thermal and RF performance on GaN/Diamond HEMT devices: reducing the operating junction temperature by 40-45% and tripling the areal RF power density compared to GaN-on-SiC [2][3][4]. But most of the work were is based on small-size GaN/Diamond wafers (<4-inch). The purpose of this work is to develop a manufacturing process using compatible, fully automated 4 inch tool set to fabricate GaN/Diamond HEMT in a compound semiconductor production facility. In this paper, the challenges of 4-inch GaN/Diamond HEMT fabrication process will be addressed and fully processed device results measured on a 4 inch GaN/diamond wafer will be discussed.

WAFER FABRICATION APPROACH

A. Challenges in GaN/Diamond wafer handling

In this work, GaN/Diamond epi wafers were produced by Element 6 and then processed at GCS using the standard existing 4 inch tool set as in a GaN/SiC and GaN/Si production line. The typical diamond substrate thickness varies from 110 to 135 um. Wafer warpage can be roughly several hundreds of microns to a few millimeters. Fig. 1 shows one of the free-standing GaN/Diamond wafer before wafer processing starts. Most automated fab tools with a vacuum chuck or pickup arms are not able to handle this kind of wafers due to the non-flatness of the wafer. A stiff carrier with strong bonding media is necessary for these tools to accept GaN/Diamond wafers. Especially, at the gate lithography (0.5 um) process step. Using a Canon stepper, wafer bowing and poor thickness uniformity presented extraordinary challenges. Special care was taken to overcome the tool handling and auto focus/tilt issues. To address these challenges, a number of temporary wafer bonding techniques we evaluated against: bonding temperature tolerance, chemical resistance, and tool handling compatibility. In the end, wafers could be processed through the entire front side process on the existing tool set.

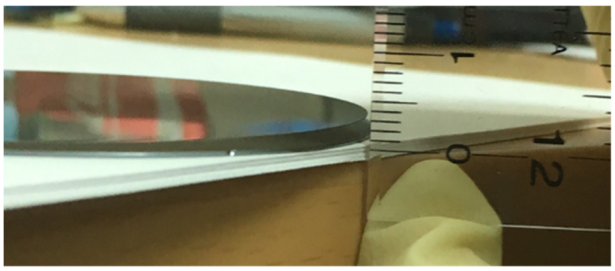


Fig.1 Free-standing GaN/Diamond wafer bowing (warpage) of several millimeters as measured using a ruler,

B. Wafer bonding techniques and carrier selection

An ideal wafer bonding technique for GaN/Diamond wafers must withstand various process chemicals, plasma conditions, and process temperatures. Several different approaches were attempted and evaluated initially. These included: electrostatic bonding, adhesive tape bonding, polymer adhesive bonding, etc. It was quickly concluded that none of the techniques evaluated could survive the entire process sequence. A flexible approach using combination of

several techniques, involving several bonding/de-bonding steps, was found to work better.

The carrier material for wafer bonding is critical to the success of wafer handling. Several factors have to be considered when selecting carriers for this purpose:

- Cost and availability
- TCE compatibility with diamond
- Thickness and strength
- Chemical compatibility with process

Si and sapphire substrates are the most common and relatively inexpensive carriers in the semiconductor fab. However, their TCE is worse than diamond and not robust across all manufacturing processes. In the first few attempts of bonding with diamond wafers, they worked fine for low temperature processes. But when the process temperature requirement approached 200 °C, the carrier or the wafer cracked in thermal cycling. In some cases, the bow characteristics of the GaN/Diamond wafer transferred to the carrier wafer and the bonded sandwich. Fig, 2 shows a bow measurement data (~200um) of a bonded sandwich while the carrier had an initial bow of less than 1 um. Based on numerous trials and evaluation results, a flexible combination approach was adopted. The final process utilized a Si carrier for low temperature, temporary bonding and a SiC carrier for processes involving higher temperatures. For very high processing temperatures (RTA > 400 °C), no wafer bonding is used.

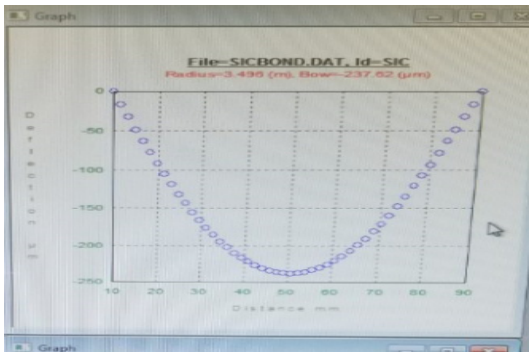


Fig 2. Bow measurement data of a bonded sandwich using a SiC carrier.

C. GaN HEMT process flow

The standard GaN/SiC process flow at GCS, starts with high temperature ohmic alloying, SiN deposition and implant isolation to define the active layer. Gate formation involves a gate SiN etch then a gate metal deposition and anneal. This is followed by a 2nd SiN layer, which is deposited to passivate the gates. M1 interconnect, 3rd SiN layer and air bridge follows to complete the upper layers of the device. Fig. 3 illustrates the simplified process flow. GaN/Diamond wafers basically follow the same process route with slight variations in some process parameters due to their different thermal behaviors when bonded on a carrier. In Fig 4, a 4-inch GaN/Diamond HEMT wafer is shown with front side processing completed in the 4-inch compound semiconductor production line, which includes source and drain ohmic contacts, device isolation, surface passivation, 0.5um gate formation, a source-connected field plate, and plated air bridges.

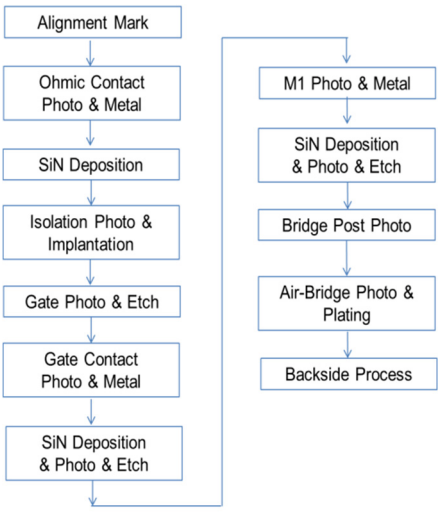


Fig.3. Standard GaN/SiC Process Flow

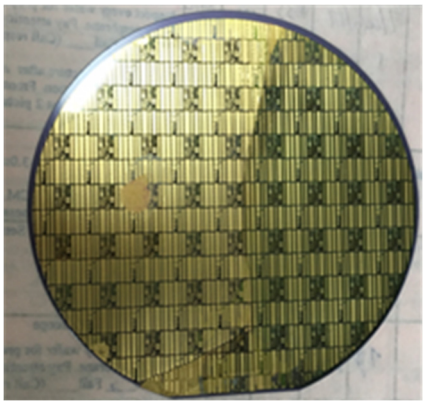


Fig 4. Full 4 inch GaN/Diamond wafer with The front side processing completed.

DEVICE FABRICATION RESULTS

In the very first run of the GaN/Diamond process, a mysterious leakage current caused devices to show relatively poor RF performance. A separate DOE was immediately conducted in order to understand the origin of the leakage current, which will be discussed in the following section.

A. *Surface leakage issue*

Since standard isolation implants of multiple energies were applied to both GaN/Diamond and GaN/Si wafers shown in Fig. 5, we believe the origin of the mysterious leakage current in GaN/Diamond, most likely was due the surface preparation during the diamond CVD process. Further DOE results indicated the leakage was caused by the interface charges on top surface of the GaN epi during the epi-flip process. The standard isolation implant process was found not to be effective in reducing this leakage current. However, with further process optimization, a proprietary surface treatment successfully removed the extra leakage current. As a result, excellent leakage currents were obtained (same level as typical GaN/Si) without adversely affecting channel current (from 2-DEG). Fig. 6, illustrates mesa-to-mesa leakage current obtainable from the optimization DOE, which is at a similar level to typical GaN/Si and GaN/SiC wafers.

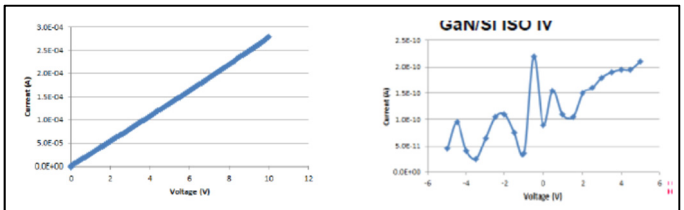


Fig. 5 Mesa-to-mesa leakage current comparison as measured after isolation implant for the 1st run of GaN/Diamond (left) and a typical GaN/Si wafer. The former is several orders of magnitude higher than the latter.

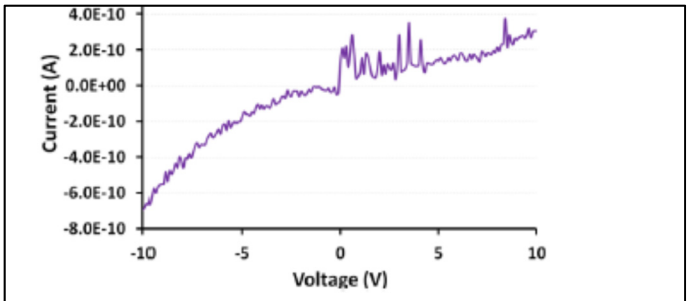
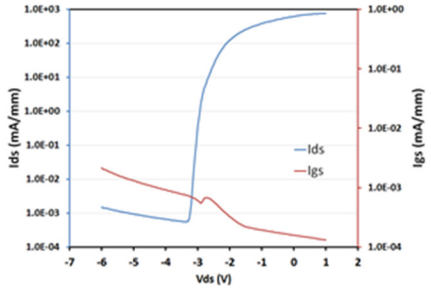


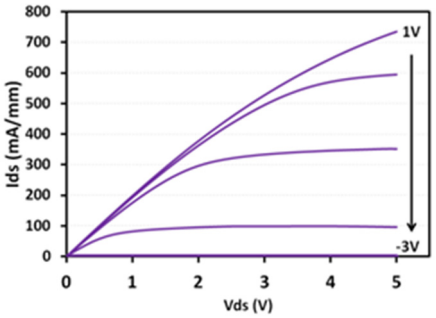
Fig. 6 Excellent mesa-to-mesa leakage current was obtained after process optimization.

B. *On-wafer DC/RF measurement result*

Fig. 7 shows a typical I-V and transfer characteristics of GaN/Diamond HEMT. The device periphery is 2x80um with 0.5um gate length. As shown in the I-V plots, the device demonstrates very low gate leakage current and OFF-state drain leakage current. Saturation current density of the device is typical for a GaN/Si HEMT of a comparable epi structure. An On/Off ratio of 10^6 was obtained, similar to typical GaN/SiC and GaN/Si devices.



(a) Transfer curves



(b) Family I-V curves

Fig. 7 Wafer level DC test results from a 4 inch GaN/Diamond wafer measured at front side completion. (as) shows the transfer curves and (b) highlights the I-V family curves.

On-wafer RF small signal and load pull (2GHz) measurements were conducted on planar 2-finger devices (2x80 um). A representative load-pull data set showing gain and out power for Vds = 28V, 40V and 50V are plotted in Fig. 8. The device delivered a power density of 7.8 W/mm at Vds =50V at 2 GHz, which is comparable to a typical GaN/SiC HEMT device.

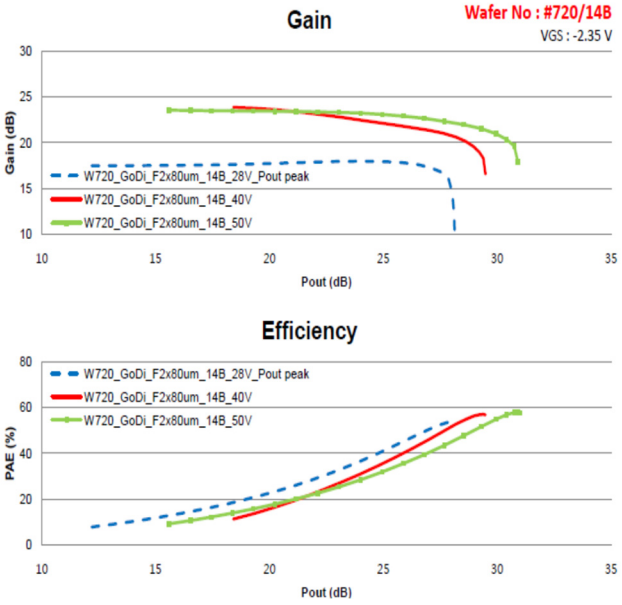


Fig.8 On-wafer load-pull data of a 0.5um device (2x80 um) at Vds = 28V, 40V, 50V

C Thermal Characteristics

To further evaluate the thermal characteristics of GaN/Diamond devices, larger multi-finger devices will be packaged and tested. Surface temperature of these devices under bias can be measured with an IR microscope. GCS believes the advantage of GaN/Diamond, will show up more clearly in the large device package tests planned for future studies.

PLAN FOR WAFER THINNING AND BACKSIDE VIAS

Diamond is the hardest material in the world, typical wet chemicals and dry etch techniques such as RIE and ICP etch are not practical for deep via formation. These etch rates range from nothing to very small. The only feasible approach to form deep via holes is laser drilling using short wavelength lasers. Our initial test of such laser drilling techniques demonstrated high enough drilling rates, warranting further exploration. The challenge is that laser drilling process is nonselective. When drilling from the backside of diamond wafer, the drilling process will not stop when it hits the front side metal as in a normal RIE or ICP etch process. It would simply punch a hole in the front side metal pad. On the other hand, if drilling from the front side first, through holes in the diamond substrate will make front side pads and via patterning/metallization process very difficult or nearly impossible.

The plan is to use a laser to drill combine with front side & back side hole at different process step followed by front side & back side Au plating process. The combined process is currently in development.

CONCLUSIONS

The need for 4 inch GaN/Diamond fabrication in parallel with current GaN/SiC and GaN/Si production presented a unique set of challenges to engineers. In this work, these challenges were overcome and a successful fabrication process of GaN/Diamond wafers was demonstrated. Wafer-level measurements showed DC/RF device performance comparable to those obtained from GaN/SiC counterparts. Backside via formation process remains as challenge to be resolved in future work.

ACKNOLEDGEMENT

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