Performance and Manufacturing Perspectives of SiC T-MOSFET Devices

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Abstract

For SiC power switches the MOSFET concept is favored over other device forms like JFET and BJT since it is normally-off and voltage controlled. The market introduction started with lateral DMOS MOSFETs in the 1200V class and currently is expanding to higher voltage classes. The first 1200V trench (T)-MOSFETs have been introduced [1]. This paper will discuss the performance benefits and manufacturing challenges of these devices. SiC MOSFETs are suited to be utilized in a broad spectrum of applications, such as Photovoltaic, UPS, drives, and traction.

INTRODUCTION

In order to discuss the processing of SiC MOSFETs it is best to focus on the MOS channel which is the most demanding device element. In contrast to Si based high voltage MOS transistors, the channel of SiC devices adds a major portion of the overall on-resistance. Hence, the challenge in designing a proper SiC MOSFET transistor is to enable a sufficiently high channel conductance $\boldsymbol{G_{cha}}$ which can be calculated for small $\boldsymbol{V_{DS}}$ by:

$$G_{cha} = \frac{w}{L} \mu_{FE} \frac{\varepsilon_{ox}}{t_{ox}} \left(V_{GS} - V_{th} \right) \qquad (1)$$

One has to concentrate on four major influence factors in designing a good device: (i) minimize the gate oxide thickness $\boldsymbol{t_{ox}}$ with guaranteed reliability, (ii) maximize the channel density (width $\boldsymbol{w}$ per device area), (iii) minimize the channel length $\boldsymbol{L}$ for the desired blocking capability and (iv) maximize the field effect mobility $\boldsymbol{\mu_{FE}}$. By simply applying trench technology two restrictions of the lateral DMOS concept are already improved: (i) field effect mobility $\boldsymbol{\mu_{FE}}$ can be increased by taking advantage of the orientation dependence and (ii) the limitation of channel density $\boldsymbol{w/A_{act}}$ for lateral devices can be overcome. This step has similarly been taken years ago in the development of Si power MOSFETs. This paper will discuss the implementation of this structure in SiC. Furthermore, state of the art Si based power transistors will be compared by means of general differences between Si and SiC processing. Finally, a processing overview of Infineon's MOSFET (trademark CoolSiC™) as depicted in Fig. 1 will be provided.

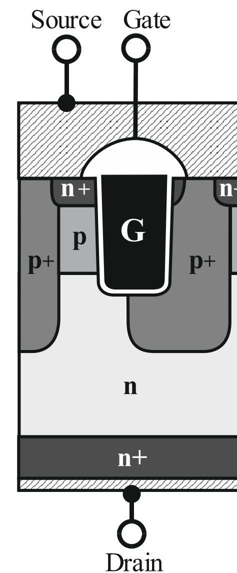

Figure 1: Sketch of the trench SiC MOSFET cell

SIC T-MOSFET

The performance of this new T-MOSFET concept as described in [2, 3 and 5] allows one to cut the specific on-resistance $\boldsymbol{R_{DS(on)}*A_{act}}$ by nearly half compared to an equivalent DMOS without compromising GOX reliability or $\boldsymbol{V_{th}}$. This is achieved by employing the MOS channel on the a-plane of the SiC crystal structure. Previously it has been shown that the mobility for this crystal plane is about two times higher compared to other crystal planes [4]. In general,

it is a challenge for a MOSFET structure to trade-off between JFET resistance and the gate oxide field. Hence, for trench devices one needs to utilize deep p-well structures. State of the art implantation techniques allow an accurate depth control. In order to overcome the problems of lateral alignment some concepts implant self-aligned through the trench opening to achieve the depth. The standard method to form the SiC trenches is to use oxide hard masks with dry-etching. Fig. 2 shows the SEM cross section of a trench typically used in a T-MOSFET. Different techniques based on dry and wet etching combined with sacrificial oxidation were adapted from Si device processing in order to define the final shape of the trenches. Furthermore, an adequate rounding of the corners is an important design parameter to minimize the gate oxide field stress. In addition, the position of the trench with respect to the p-wells affects the performance of the device.

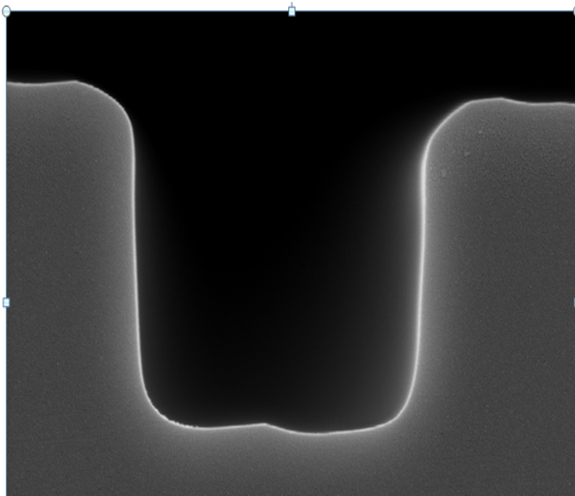

Figure 2: Typical SEM cross section of the trench profile

Conclusions

In summary, the use of a T-MOSFET not only enables higher performance devices but also requires higher effort in process technology compared to lateral devices. Various process parameters, such as sidewall shape accuracy, critical dimensions, line width and alignment tolerances, as well as the control of the vertical dimensions have to be controlled intensively. The challenge to produce T-MOSFETs is tackled by the successful development of many sophisticated processes, by strong process integration experience and deep know-how of a Si line established for high volume fabrication. For next generations of SiC T-MOSFETs the path is open to scale down the pitch and thereby improve the performance of the devices.

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Acronyms

SiC: Silicon Carbide
MOS: Metal Oxide Semiconductor
FET: Field Effect Transistor
JFET: Junction Field Effect Transistor
SEM: Scanning Electron Microscopy