Developments of Ga_2O_3 Electronic Devices for Next-Generation Power Switching

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Abstract

Gallium oxide (Ga_2O_3) has been gaining considerable attention as a representative of ultra-wide bandgap semiconductors. This paper introduces our state-of-the-art Ga_2O_3 device technologies developed for applications to future power switching electronics.

Introduction

In the past five years or so, gallium oxide (Ga_2O_3) has been recognized as a new ultra-wide bandgap semiconductor and become an active R&D field [1]. The motivation for device development is often inspired by its unique material properties based on the extremely large bandgap of 4.5 eV [2] and availability of large-size, high-quality, affordable single-crystal wafers produced from melt-grown bulks [3]. However, Ga_2O_3 electronic devices are still at a primitive stage of R&D and thus remain far less mature than GaN and SiC devices. We have been pursuing pioneering R&D of Ga_2O_3 transistors and diodes, and significant progress has been made in the last few years.

In this paper, we will present our current Ga_2O_3 MOSFET and SBD technologies developed for applications to power electronics.

Ga_2O_3 MOSFET

Lateral Ga_2O_3 MOSFET

Figure 1 shows a schematic cross section of a lateral Ga_2O_3 MOSFET with an FP [4]. An unintentionally-doped Ga_2O_3 layer with a thickness of 300 nm was grown on an Fe-doped semi-insulating β-Ga_2O_3 (010) substrate by molecular beam epitaxy. The n-Ga_2O_3 channel layer and n^+-Ga_2O_3 ohmic regions were fabricated by employing Si-ion (Si^+) implantation doping. The implanted Si atom densities in the channel layer and the ohmic regions were 3×10^{17} and 5×10^{19} cm^{-3}, respectively.

Figure 2 shows DC drain current–voltage (I_d–V_d) characteristics at room temperature. The maximum I_d was 78 mA/mm at a gate voltage (V_g) of +4 V, and an off-state breakdown voltage (V_{br}) reached to 755 V. A leakage I_d in the off-state was less than lower limitation of our measurement setup, leading to a large I_d on/off ratio of over nine orders of magnitude. From comparison between DC and pulsed I_d–V_d curves as shown in Fig. 3, it turned out that the FP-MOSFETs showed negligibly small DC–RF dispersion in output characteristics. Stable high-temperature operation was confirmed up to 300°C; I_d–V_d characteristics evolved smoothly with no kink or abrupt change in behavior by increasing operation temperature.

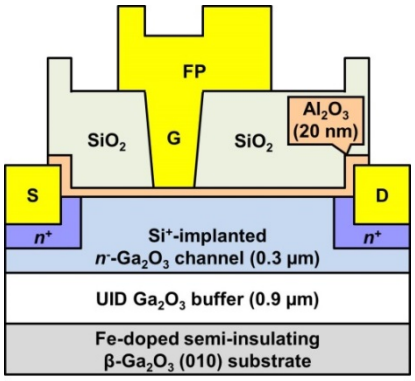

Fig. 1. Schematic cross section of lateral Ga_2O_3 FP-MOSFET.

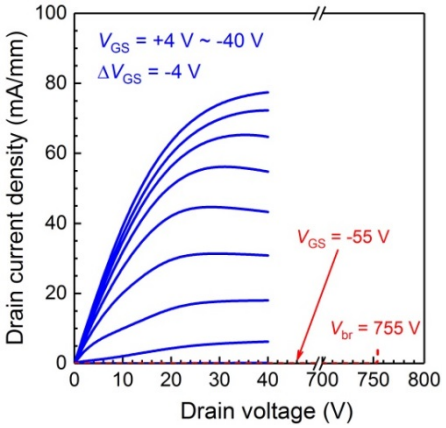

Fig. 2. DC I_d–V_d characteristics of lateral Ga_2O_3 FP-MOSFET.

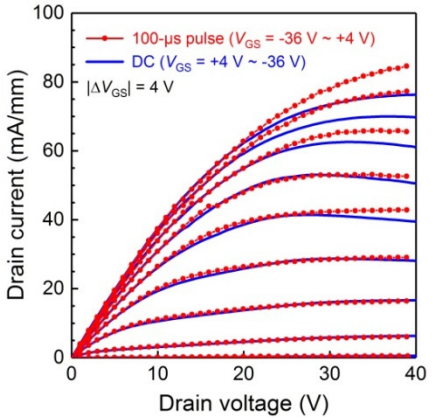

Fig. 3. Comparison between DC and pulsed I_d–V_d characteristics of lateral Ga_2O_3 FP-MOSFET.

Single-crystal Ga_2O_3/polycrystalline SiC bonding wafer

We characterized the channel temperature in the FP-MOSFET by comparing pulsed I_d–V_d with DC one, together with device simulation [5]. A large thermal resistance of 48 mm·K/W was extracted at room temperature as expected from the low thermal conductivity of Ga_2O_3, indicating that efficient heat extraction from the active region will play a critical role in improving device performance and reliability.

To solve the poor heat dissipation issue of Ga_2O_3 devices during high-power operation, we recently developed direct wafer-bonding technology of a single-crystal Ga_2O_3 and a polycrystalline SiC [6]. Figure 4 shows a photograph of a single-crystal Ga_2O_3/polycrystalline SiC bonding wafer. The wafer had a large bonding strength at the interface, which was at least comparable with the Ga_2O_3 bulk strength. The effective thermal conductivity of the bonding wafer increases with decreasing the Ga_2O_3 thickness as shown in Fig. 5 and reaches to values comparable with those of Si and GaN at the thicknesses of about 20 and 10 μm, respectively. We also confirmed that the electrical conductivity at the bonding interface was sufficiently small. These results indicate that the wafer bonding can be one of the effective techniques for future developments of high-power Ga_2O_3 devices.

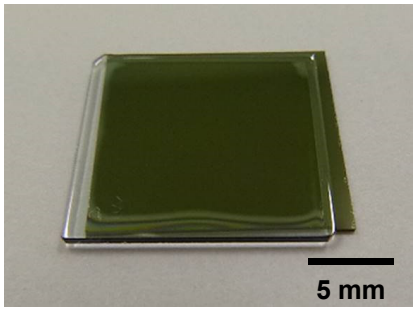

Fig. 4. Photograph of single-crystal Ga_2O_3 (upper, 630-μm thick)/polycrystalline SiC (lower, 350-μm thick) bonding wafer.

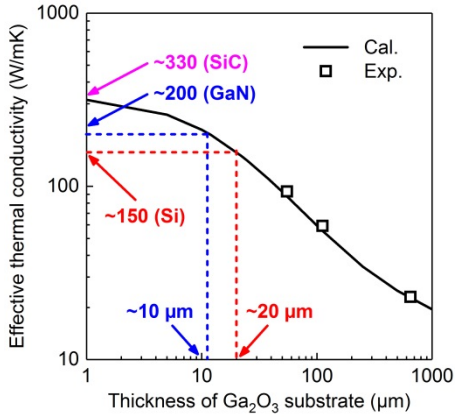

Fig. 5. Ga_2O_3 thickness dependence of effective thermal conductivity of the bonding wafer. The solid line is given by the following equation:
$\lambda_{total} = (t_{Ga2O3} + t_{SiC}) / (t_{Ga2O3}/\lambda_{Ga2O3} + t_{SiC}/\lambda_{SiC})$,
where λ is the thermal conductivity, and t is the thickness.

Vertical Ga_2O_3 MOSFET

For high-voltage and high-power applications, vertical device structures are preferred since they can utilize the device chip area more efficiently than the lateral devices. Recently, we fabricated vertical depletion-mode Ga_2O_3 MOSFETs schematically illustrated in Fig. 6 [7]. A Si-doped n^--Ga_2O_3 drift layer with an electron density (n) of 3×10^{16} cm^{-3} was grown on a Sn-doped n^+-Ga_2O_3 (001) substrate by HVPE. In the vertical MOSFET structure, the source was electrically isolated from the drain by a current blocking layer except at an aperture opening through which I_d was conducted. The current blocking layer was fabricated by Mg-ion (Mg^{++}) implantation doping, followed by the activation annealing at 1000°C in N_2 gas atmosphere. Both Si-doped n-Ga_2O_3 channel (Si=3×10^{17} cm^{-3}, 0.3-μm-thick box profile) and n^{++}-Ga_2O_3 source contact regions (Si=5×10^{19} cm^{-3}, 0.15-μm-thick box profile) were formed by implantation doping, as was the case of the lateral FP-MOSFETs. A 50-nm-thick Al_2O_3 gate dielectric was then formed by plasma atomic layer deposition and patterned for source electrode window openings. Annealed Ti/Au was used for the source/drain ohmic electrodes, while Ti/Pt/Au formed the gate electrode.

Figure 7 shows the room-temperature DC I_d–V_d characteristics of the vertical MOSFET with a gate-source spacing of 5 μm, a source width of 200 μm, a gate-current blocking layer overlap of 2.5 μm, an aperture length of 15 μm, and an aperture width of 200 μm. Despite a large I_d leakage due to the imperfect function of the blocking layer, the small I_d modulation by V_g swing was demonstrated. Transfer characteristics measured at V_d=8 V yielded a peak transconductance of 1.25 mS/mm. Improvement of the current blocking layer is the most important technical challenge for the next device process.

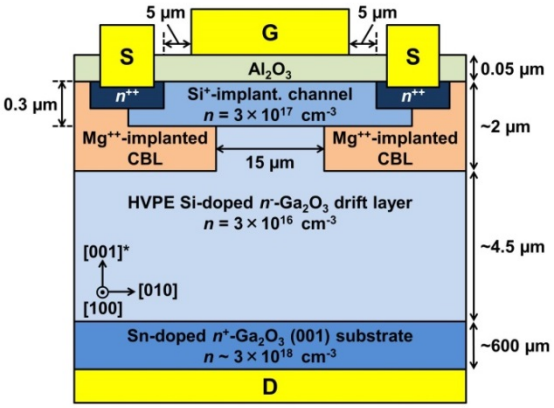

Fig. 6. Schematic cross section of vertical Ga_2O_3 MOSFET.

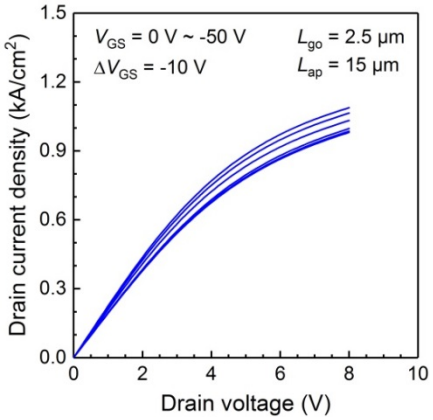

Fig. 7. DC I_d–V_d characteristics of vertical Ga_2O_3 MOSFET.

Ga_2O_3 SBD

Ga_2O_3 FP-SBDs were fabricated on a Si-doped n^--Ga_2O_3 drift layer grown on a Sn-doped n^+-Ga_2O_3 (001) substrate by HVPE [8]. Figure 8 shows a schematic cross section of the FP-SBD. 200-μm-diameter Pt/Ti/Au Schottky FP-anode and Ti/Au ohmic cathode electrodes were formed on front and back sides of the substrate, respectively. The net donor concentration of the drift layer was estimated to be 1.8×10^{16} cm^{-3} by capacitance–voltage measurement.

The room-temperature current density–voltage (J–V) characteristic is shown in Fig. 9. From the forward J–V characteristics, the specific on-resistance and the ideality factor were estimated to be 5.1 mΩ·cm^2 and 1.05, respectively. Successful FP engineering resulted in an off-state V_{br} of 1076 V. From device simulation at the breakdown condition, the maximum electric fields in the Ga_2O_3 drift layer under the anode foot and the FP edge were analytically extracted to be more than 5 MV/cm, which is much larger than the theoretical limits for SiC and GaN. Stable device operation at both forward and reverse biased conditions was maintained even at elevated temperatures up to 200°C.

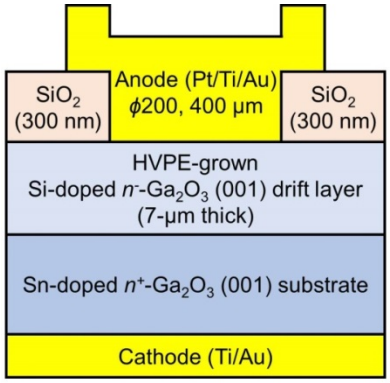

Fig. 8. Schematic cross section of vertical Ga_2O_3 FP-SBD.

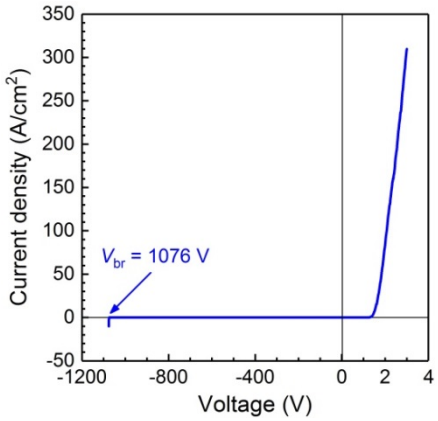

Fig. 9. DC J–V characteristics of vertical Ga_2O_3 FP-SBD.

Conclusions

We fabricated and characterized Ga_2O_3 lateral FP-MOSFETs, vertical MOSFETs, and vertical SBDs. Their device characteristics were reasonably good for the relatively simple device structures, indicating their large potential for applications to future power electronics.

Acknowledgements

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References

[1] J. Y. Tsao et al., Adv. Electron. Mater. 4, 1600501 (2018).
[2] T. Onuma et al., Jpn, J. Appl. Phys. 54, 112601 (2015).
[3] A. Kuramata et al., Jpn, J. Appl. Phys. 55, 1202A2 (2016).
[4] M. H. Wong et al., IEEE Electron Device Lett. 37, 212 (2016).

[5] M. H. Wong et al., Appl. Phys. Lett. 109, 193503 (2016).
[6] N. Hatta et al., *Direct bonding of gallium oxide and polycrystalline silicon carbide substrates using Surface-Activated-Bonding method*, 2nd International Workshop on Gallium Oxide and Related Materials (IWGO-2) Abstract, September 2017.
[7] M. H. Wong et al., *First Demonstration of Vertical Ga_2O_3 MOSFET: Planar Structure with a Current Aperture*, 75th Device Research Conference (DRC 2017) Technical Digest, June 2017.
[8] K. Konishi et al., Appl. Phys. Lett. 110, 103506 (2017).

ACRONYMS

R&D: Research and Development
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
SBD: Schottky Barrier Diode
FP: Field Plate
HVPE: Halide Vapor Phase Epitaxy