Enhancing the Manufacturability and Evolving the Technology of GaN on SiC Back-Side Vias

Chia-Hao Chen, Yu-Wei Chang, Shih-Hui Huang, Fraser Wang, Benny Ho, Walter Wohlmuth

WIN Semiconductors Corp, No. 35, Technology 7th Road, Hwaya Technology Park,
Kuei Shan Hsiang, Tao Yuan Shien, Taiwan 333
walterw@winfoundry.com, Tel +886 3 3975999 ext 1141

Keywords: GaN on SiC, MMIC, RF

ABSTRACT

Creating a manufacturable back-side via process is a key challenge for achieving high-yield GaN MMICs however process evolution requires enhancements to existing processes. The back-side via was shrunk from 85µm diameter, circular to 30x60 µm oval vias to enable integrated source vias within the transistors, a non-wet film lining the vias to prevent AuSn die attach ingress into the via was implemented, a change of the front-side etch stop metal to improve reliability was implemented, and the use of very thin layers of GaN-based epitaxy upon which the back-side via etch is required to stop on was enabled. These improvements were done in parallel with improving utilization in regards to cycle time and throughput, improving back-side via sidewall profile and improving back-side edge exclusion from 7 to 5 mm.

INTRODUCTION

The mass production of GaN HEMTs on SiC substrates for RF commercial and defense markets have continued to grow with advances in manufacturing, yield improvement, and technology innovation led by volume production of GaN for base station, fixed infrastructure markets as GaN on SiC displaces the incumbent Silicon LDMOS technology. A majority of these RF devices require the use of back-side vias for low inductance and low resistance source connections to RF integrated circuits and power cells. Significant progress was made in creating back-side vias in GaN on SiC materials that are pillar free through etch optimization and byproduct free through cleaning optimization [1]. Once a repeatable baseline process was establish then refinements of the process where undertaken in the areas of optimizing the shape of the back-side via, shrinking the via from 85µm diameter, circular to 30x60 µm oval shaped, changing the front-side contact metal, thinning the GaN-based materials, improving cycle time and throughput, and enabling non-wetting material lining to prevent AuSn eutectic encroachment into the via during die attach processes required for packaging. In this paper, these topics concerning the advancement and improved manufacturability of through wafer vias in GaN on SiC will be addressed.

EXPERIMENTAL

Upon completion of the front-side process to form the transistors, MMICs and interconnect structures the GaN/SiC processed wafers are temporarily bonded face down to an n-type SiC carrier by using a proprietary liquid wax which has a cure temperature in excess of 150°C. Re-usable n-type SiC substrates are implemented as temporary carriers during back-side processing as they are well-matched to S.I. SiC substrates in regards to thermal expansion co-efficient, transparency for front- to back-side alignment, and thermal conductivity. The high temperature liquid wax enables the SiC etch process to run at higher power resulting in faster etch rates improving cycle time. The GaN on SiC wafer is ground to a target 100 µm thickness. The thickness of each wafer is recorded in the electronic manufacturing systems (EMS) and the information is feed forward to the SiC etch equipment which picks individual recipes for each wafer based on the ground wafer thickness to optimize cycle time and throughput. The SiC etch is a 2-step etch with a fast, first etch that removes a majority of the SiC followed by a slow, second etch that gently stops on the GaN-based epitaxy. The GaN layer was then etched, using the SiC substrate as the mask, stopping on the front-side metal. The front-side metal was changed from Ohmic to Metal0 as the process matured. The Aluminum in the Ohmic metal can contribute to forming an electro-chemical cell during substrate via cleaning causing degradation in yield whereas inert TiPtAu-based metal within Metal0 is more robust.

RESULTS

The use of 85 µm diameter, circular back-side vias used in the past are not practically feasible when considering creating a transistor with integrated source via (ISV) topology. The standard outside source via (OSV) transistor provides good performance at low frequency but parasitic source inductance and resistance limits performance at higher frequencies. All back-side vias were changed from 85 µm circular vias to 30x60 µm

oval vias to enable a compact ISV transistor cell and to avoid having different sized vias processed at the same time due to loading effect concerns during etching.

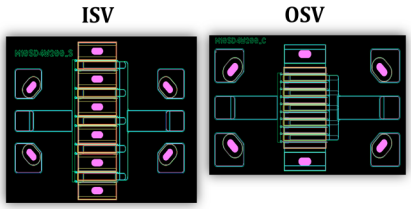

Fig.1 ISV and OSV transistor layouts options

The etching rate for the 30x60 µm oval vias is slower than the 85µm diameter, circular vias. The SiC main etch, etch rate reduced from 1.2 to 1.0 µm/min and the SiC secondary etch, etch rate reduced from 1.0 to 0.8 µm/min. The process time increased from 2.0 hours to 2.5 hours for standard epitaxy that utilizes a 2.0 µm total thickness of GaN-based epitaxy.

The sidewall profile of the back-side vias was improved by increasing the electroplated Ni hard mask metal thickness from 4.5 to 10 µm [1]. Etch byproducts are seen on the sidewalls after the SiC etch, as shown in Figure 2.

Fig.2 ISV back-side via cross-sectional SEM after SiC etch with the Ni-based hard mask not yet removed

The SiC secondary etch was tuned to minimize etching (< 0.3 µm) of the GaN-based epitaxy with good run-to-run and center-to-edge reproducibility. The areas in the blue boxes in the SEM in Figure 2 are shown in a zoomed in SEM in Figure 3. The sidewall transition is sharp with no notches or residual SiC.

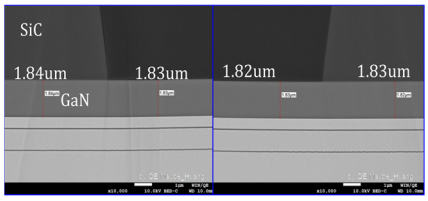

Fig.3 ISV back-side via cross-sectional SEM after SiC etch zoomed in to see the GaN epitaxy and the SiC sidewall

Detailed inspection of the back-side vias after etch byproduct cleaning was performed using 3D x-ray imaging to ensure the vias were residue free as shown in Figure 4.

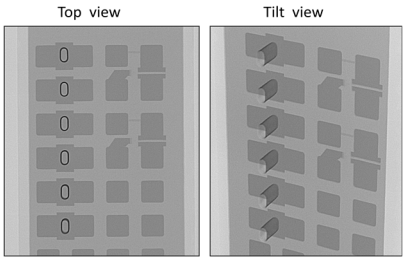

Fig.4 Top or plan view and tilt view of 30x60µm oval vias after etch and cleaning completion.

A seed layer of Ti/TiW/Au was sputter-deposited in a high-field chamber to ensure good sidewall coverage into the depths of the vias then 5µm of electroplated Au was formed on top of the seed layers achieving >3µm of Au along the depth of the via.

The front-side landing pad for the back-side via etch was changed from Ohmic metal to Metal0 as the Aluminum in the Ohmic can be etched through electrochemical processes during the via cleaning process causing reliability and yield problems.

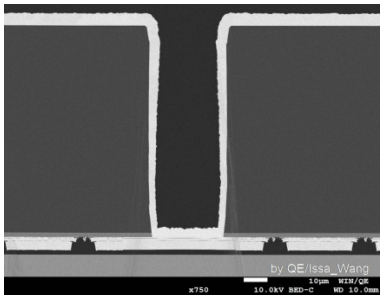

Fig.5 1SV back-side via cross-sectional SEM after metallization

A majority of customers desire to have AuSn eutectic die attach to a Cu-based heat sink. The use of a non-wet film to line the inside of the back-side via and extend 10-15 µm past the edge of the via prevents the Sn in the AuSn from entering the via during die attach and potentially causing reliability concerns due to Sn migration into the front-side and into the transistor. The non-wet Ta film is now incorporated into all of our standard GaN processes.

The standard 2 µm GaN-based epitaxy layer thickness formed our initial GaN technology basis, but as the technologies matured so did the epitaxy design pushing the GaN-based epitaxy layer thickness down to 0.5 µm in some cases. The thinned GaN-based epitaxy presented difficulty in achieving a soft landing, into the GaN materials during the SiC overetch. If the SiC etch breaks through the GaN-based epitaxy or cracks form through the GaN-based epitaxy then the strong acids used for cleaning the Ni-based byproducts out of the vias after SiC etch can etch the front-side metals. Optimization of the main and secondary etch steps were required for the thinner epitaxy. The source power and bias for the secondary etch of the SiC were significantly reduced slowing down the etch time of the secondary etch from 2 hours to 6 hours for the 2.0 to the 0.5 µm thick GaN-based epitaxy, respectively.

To reduce the etch time we implemented 2 critical changes. The first was to create a feed-forward system

for variations in substrate thickness after back-side grinding. The substrate thickness was measured and binned into intervals of 1µm from 97 to 103 µm thickness and each bin had a specific main etch recipe. The measurement data for ground wafer thickness was input into the MES SiView system and the ICP tool would automatically select the specific recipe for the bin. This binning enables the main etch to etch deeper into the SiC prior to switching to the secondary etch. The main etch depth was changed from 93 to 97 µm or 7 to 3 µm of material remaining. These 2 changes enabled SiC overetch etch time to be reduced from 6 to 4 hours for 0.5 µm GaN-based epitaxy with a small increase of 73 to 78 min for the SiC main etch. Further improvements to cycle time are being developed by increasing the source power, bias power, and the pressure to shorten the secondary etch step to less than 2 hours.

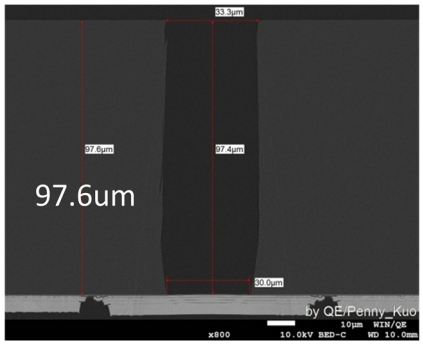

Fig.6 ISV back-side via cross-sectional SEM after SiC etch with GaN-based epitaxy thickness of 0.5µm.

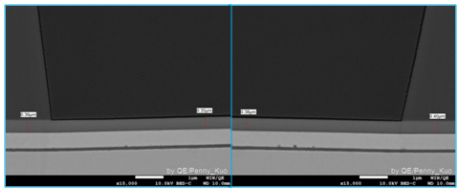
Fig.7 ISV back-side via cross-sectional SEM after SiC etch zoomed in to see the thin GaN epitaxy and the SiC sidewall

The wafer plus carrier are placed onto the electrostatic chuck with the SPTS APS tool and held in place with a weighted wafer edge protection (WEP) mechanical clamp to ensure that the wafer plus carrier remain flat during ICP etching at elevated temperatures [2]. The WEP inner diameter was altered from 91 to 95 mm to enable back-side vias out past 5 mm edge exclusion to be straight instead of tilted by enhancing the cross-wafer plasma uniformity.

CONCLUSIONS

Improvements to a GaN on SiC back-side via process has been shown with enhancements to the sidewall SiC profile, enablement of using thin GaN-based epitaxy, increased throughput through process tuning and MES binning, and more useable die per wafer by reducing the exclusion zone.

ACKNOWLEDGEMENTS

The authors would like to thank all of the staff at WIN Semiconductors who supported the GaN technology development.

REFERENCES

[1] Chia-Hao Chen, Yu-Wei Chang, Ming-Hung Weng, Ricky Chang, Shih-Hui Huang, Fraser Wang, Yi-Feng Wei, Stanley Hsieh, I-Te Cho, Walter Wohlmuth, *Method for Forming Through Wafer Vias in GaN on SiC Devices and Circuits*, 2014 CS MANTECH Technical Digest, pp. 275-278, May 2014

[2] Chia-Hao Chen, Yi-Feng Wei, Yao-Chung Hsieh, I-Te Cho, Walter Wohlmuth, *Wafer Edge Protector*, US Patent Application 20140283991.