Design of Graded AlGaN Channel Transistors for Improved Large-Signal Linearity

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Abstract

We report on the design of graded AlGaN channel HEMTs for improved two-tone linearity. Bias dependent small-signal characteristics were extracted from 2D device simulations and used to estimate linearity performance using large-signal harmonic balance simulations. We investigated the potential of linearly graded AlGaN channel polarization-doped field-effect transistors (PolFETs) for high power, high linearity applications. Detailed large signal harmonic balance simulations show that PolFETs provide at least 5 dBc better IM3 suppression than standard abrupt junction GaN/AlGaN high electron mobility transistors (HEMTs) over a very wide range of output power.

Introduction

Future military and commercial communication applications require high linearity sources and receivers at high frequencies. Power amplifier linearity improvements can be achieved either at the circuit level or through improvements in intrinsic device design. While circuit level methods for linearity improvement exist, direct improvement of the linearity by device level design to reduce distortion is gaining increased attention [1]. Since device linearity at RF frequencies has a complex dependence on various parameters, detailed large signal modeling is essential to predict linearity performance of existing designs and to explore new designs that can enable improved linearity.

Currently GaN based high electron mobility transistors (HEMTs) have excellent high-power density for telecommunication applications [2]. However, existing AlGaN/GaN HEMTs are known to have gain compression as well as significant non-linearity, especially at higher operation frequencies [3]. One of the methods to mitigate the non-linearity of such transistors is to replace the conventional 2D electron gas channel with a 3-dimensional electron channel [4]. In the case of III-Nitrides, such polarization-graded field effect transistors (PolFETs) have been reported [5] to have more constant transconductance profiles. In this work we have developed a detailed model to calculate the single-tone and two-tone linearity performance of a transistor. A combination of small signal and large signal simulations is designed to accurately predict the linearity behavior of any arbitrary channel design transistor. Here, we explore the high frequency large signal linearity of graded channel designs and compare them with the conventional AlGaN/GaN HEMTs.

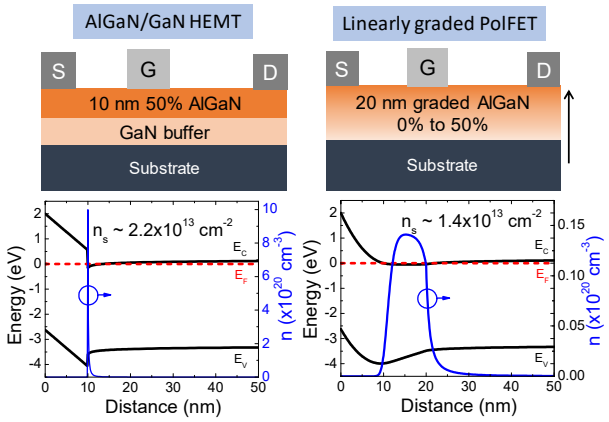

Fig. 1: Structure of the HEMT and PolFET and corresponding equilibrium band diagrams

Modeling and Simulation Setup

We compared GaN/AlGaN HEMTs with linearly graded PolFETs in terms of their C\I3 performance, i.e., fundamental signal power to third order harmonic power ratio. The structures used for the simulations are shown in Fig. 1. along with corresponding calculated equilibrium energy band diagrams. Both transistors were simulated with a gate length L_g of 250 nm, device width W of 1 mm and contact resistance R_C of 0.1 Ω-mm. The linearity performance was calculated from single-tone and two-tone simulations. The simulations were carried out by first determining bias-dependent small signal parameters using physics-based simulation, and then those small signal parameters were used to predict the linearity through large signal single-tone and two-tone simulations.

For the purpose of this work, we limited the bias dependence of small-signal input model to two parameters:

gate-source capacitance (C_{GS}) and transconductance (g_m), since these two are expected to be significantly different in the two device structures considered here. Nominal bias-dependent values for other parameters (C_{gd}, R_{out}) were chosen to be bias-independent. The general method described here can be extended to include the bias dependence of these parameters also. One-dimensional Schrödinger-Poisson calculations [6] were used for the gate-source capacitance characteristics (Fig. 2(a)), while current-voltage characteristics were simulated using Silvaco ATLAS with a density dependent saturation velocity model [7] (Fig. 2(b)).

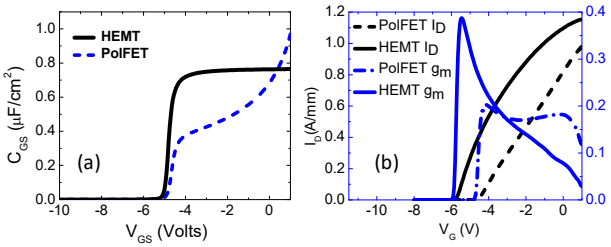

Fig. 2: Small signal simulation for HEMT and PolFET (a) C-V and (b) Transfer I-V and transconductance

The large signal simulations are done using the Keysight Advanced Design System (ADS) harmonic balance simulator. The harmonic balance setup for single tone is shown in **Error! Reference source not found.**. The small signal equivalent model takes the previously calculated I-V and C-V using the two-port Symbolically-Defined Device (SDD2P) using higher order polynomial fit within the range of operation for all bias. 10th order polynomials were found to be sufficient to match both the capacitance and transconductance individually. Separate s-parameter simulations were done to calculate the input and output impedances for each transistor. Then optimized conjugate matching circuits for maximum gains were designed using the Smith chart matching tool in ADS for each circuit at the specific bias points. To achieve the maximum linearity from each transistor, both HEMTs and PolFETs were biased as class-A amplifiers.

The harmonic balance setup for single-tone was set at a 2-GHz frequency. For the two-tone setup, the tones were separated by 10 MHz from a center frequency of 2 GHz. The load line was determined from the output I-V calculated previously using $R_L = (V_{BR} - V_K)/I_{Sat}$, where V_{BR} is the breakdown voltage, V_K is the knee voltage, and I_{Sat} is the maximum drain current. The third order intermodulation distortion (IM3) suppression for single-tone is calculated using $C\backslash I3\ (dBc) = 10\log(P_{f_1}/P_{3f_1})$, where P_{f_1} and P_{3f_1} are the power output at the fundamental f_1 frequency and the third harmonic $3f_1$ frequency respectively. For two-tone simulations, $C\backslash I3\ (dBc) = 10\log(P_{f_1}/P_{2f_{1-f_2}})$, where P_{f_1} and $P_{2f_{1-f_2}}$ are the power output at the fundamental f_1 frequency and third harmonic $2f_1 - f_2$ frequency respectively.

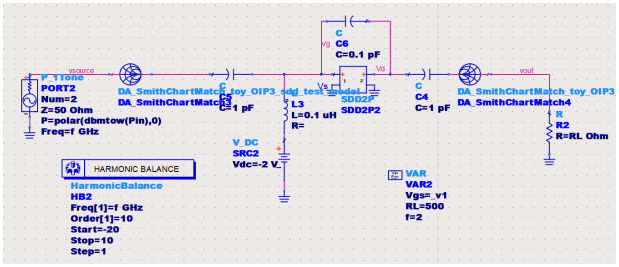

Fig. 3: ADS harmonic balance setup for single-tone measurement

Results and Discussion

Error! Reference source not found. shows the comparison between calculated single-tone performance of intrinsic third harmonic compression for HEMT and PolFET in terms of input power (P_{in}) and output power (P_{out}). Intrinsic C\I3 for the transistors are calculated with no input-output matching circuits and 50Ω load impedance in single-tone simulation, which gives an idea of the inherent non-linearity from the transistor itself only. From the figures, we can see that PolFETs are expected to give ~10 dBc higher third harmonic compression.

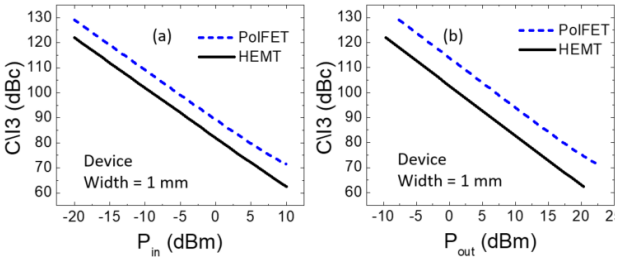

Fig. 4: Intrinsic (no-matching circuit) single-tone IM3 suppression as a function of (a) input power and (b) output power

To get the actual operating condition linearity performance of the transistors, we need to look at the transistor with matching circuits. The single-tone comparisons in terms of P_{in} and P_{out} are shown in **Error! Reference source not found.**. The PolFETs show 5-10 dBc improvement throughout the calculated range. There is a boost in the C\I3 for the PolFET of 5-10 dBm, which occurs around $V_{gs} \sim 0$ V. This is probably because both the g_m and C_{GS} are linear in a small range around $V_{gs} \sim 0$ V and hence the second derivatives are very close to zero. This makes sense as a Taylor series expansion shows that the third harmonic coefficient will

depend on the second derivative of the respective functions. The C_{GS} for the HEMT is almost constant throughout the range of operation, which shows that the output non-linearity from g_m is more dominant in the linearity performance of a transistor.

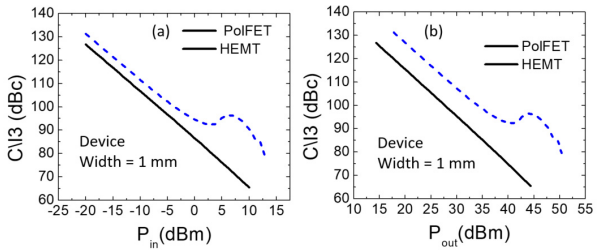

Fig. 5: Single-tone IM3 suppression as a function of (a) input power and (b) output power with optimized matching circuit

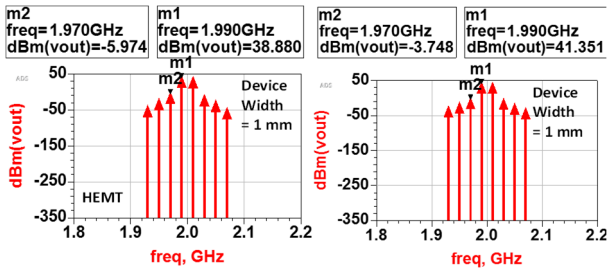

Fig. 6: Two tone simulation results to get 45 dBc IM3 suppression

Two-tone simulation results show the performance of the transistors when there are multiple closely spaced frequencies in the channel. **Error! Reference source not found.** shows the results for two-tone simulations of output power for achieving 45 dBc IM3 suppression for HEMT and PolFET separately. It shows that PolFETs (41.35 dBm) give 2.5 dBm higher output power than HEMTs (38.88 dBm) for a specified 45 dBc IM3 suppression. From multiple simulations of similar two-tone setups, available output powers to achieve some specific IM3 suppressions have been calculated. The results are shown in Fig. 7. From Fig. 7, we can see the trend of P_{out} for achieving different C\I3. At higher IM3 requirements, with decreasing output power, the PolFET performs better than the HEMT in terms of higher available output power for the same IM3 suppression.

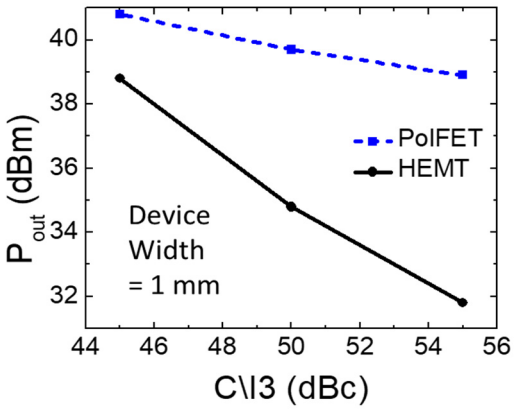

Fig. 7: Calculated output powers for different IM3 suppression values

IM3 suppressions resulting from varying output powers were calculated from two-tone simulations and the results are shown in Fig. 8. The simulations suggest that the PolFET gives 5-10 dBc higher IM3 suppression than the HEMT over most of the output power range. There is a peak in the C\I3 ratio for the PolFET in two-tone simulations also, similar to that in the single-tone case, which may be due to some cancellation of 3rd order terms due to the bias dependence g_m and C_{GS} in that range.

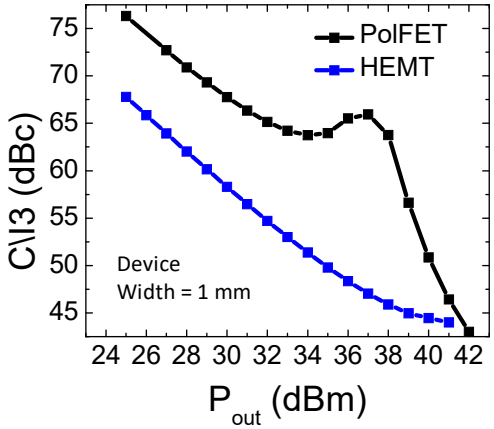

Fig. 8: Calculated output powers for different C/I3

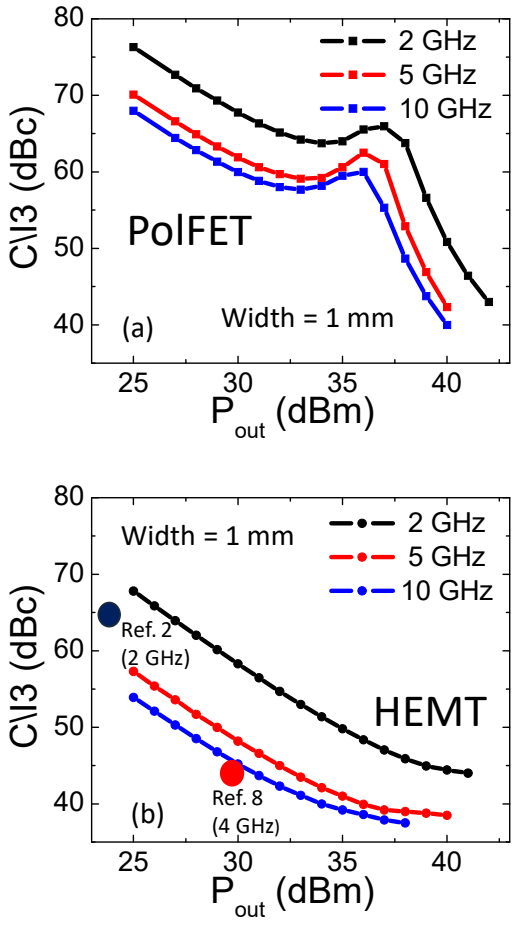

Fig. 9: Frequency effects on linearity performance of (a) PolFETs (b) HEMTs

The C_{GS} for the PolFET changes significantly over the input range of the device. This suggests that the output non-linearity due to the transconductance g_m plays a more dominant role in the linearity performance of a transistor. The nonlinearity of other device parameters will also be investigated in future work.

Figure 9 shows the dependence of the non-linearity behavior on the frequency. As the frequency increases the C\I3 decreases due to an enhancement of the non-linear terms. Experimental HEMT C\I3 values from the literature [2, 8] are also shown in Fig. 9(b) and are found to match well with the simulated values, suggesting that the assumptions made in the simulation method developed here are reasonable for predicting device performance. PolFET linearity is not reported yet in the literature. The difference in the simulated values with the experimental values are likely due to the small signal parameters which are taken to be constant (e.g., C_{gd}, R_0 etc.), which becomes more significant as we go to higher frequencies.

Conclusions

We have developed a large signal model to predict the linearity performance of novel III-Nitride channel designs. The model was used to compare the large signal linearity for conventional AlGaN/GaN HEMTs and linearly graded PolFETs. It was found that the linearly graded PolFET can be expected to provide ~5-10 dBc higher C\I3 ratio for a wide range of output power levels up to a very high-power level (~40 dBm). Our work suggests that graded AlGaN based channels could have better performance than conventional AlGaN/GaN HEMTs for telecommunication transmitter applications that require high large-signal linearity and low intermodulation distortion.

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Acronyms

HEMT: High Electron Mobility Transistor
PolFET: Polarization-graded Field Effect Transistor
C/I3: Carrier (fundamental) to Third order harmonic power ratio
IM3: Third Intermodulation Product