AlGaN/GaN MOS-HEMTs with Dual Field Plates for Stable High-Performance Operation

R. Yamaguchi, T. Yamazaki, T. Nishitani, J. T. Asubar, H. Tokuda, and M. Kuzuhara

Graduate School of Engineering, University of Fukui, 3-9-1 Bunkyo, Fukui 910-8507, Japan
e-mail: ryouta18820@gmail.com, Phone Number: +81-776-27-9714

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Abstract

We have fabricated AlGaN/GaN MOS-HEMTs with both gate and source field plates (FPs) and investigated their DC and pulsed I-V characteristics, together with the threshold voltage stability. It was found that the dual-FP MOS-HEMT exhibited the best performance both in DC and dynamic on-resistance characteristics. Furthermore, excellent stability in both positive and negative gate bias stress measurements was confirmed for the developed dual-FP MOS-HEMT. A large gate width MOS-HEMT with a chip size of 3 mm x 3 mm delivered a maximum drain current of 21 A with an off-state breakdown voltage of 950 V

INTRODUCTION

A GaN-based HEMT with a metal-oxide-semiconductor (MOS) gate is attractive for low-loss and high-power switching applications [1, 2]. Compared with the metal-semiconductor (MES) gate structure, the MOS-gate HEMT can provide a larger forward gate-to-source voltage with a reduced reverse leakage current [3]. However, several issues still remain to be solved for power switching applications such as current collapse phenomenon [4]. Use of a field plate (FP) is well-known as an efficient way to reduce current collapse in AlGaN/GaN HEMTs [5]. In this work, we have fabricated an AlGaN/GaN MOS-HEMT with both gate and source FPs, and investigated DC and pulsed I-V characteristics, together with the threshold voltage (V_{th}) stability under forward and negative gate bias stress conditions.

DEVICE STRUCTURE AND PROCESS

The cross-section of our device structure is illustrated in Fig. 1. We employed a standard AlGaN/GaN heterostructure grown by MOCVD on a SiC substrate. The AlGaN barrier layer is of 25 nm thickness with an Al content of 20%. HEMTs were fabricated with a gate length (L_g) of 3 μm and a gate-to-drain spacing (L_{gd}) of 15 μm. A gate-FP (G-FP) length and a source-FP (S-FP) length were 3 and 6 μm, respectively. Devices were passivated with a 150 nm-thick SiN film and a 400 nm-thick SiO_2 film. An ALD-Al_2O_3 film with a thickness of 10 nm was used as a gate dielectric.

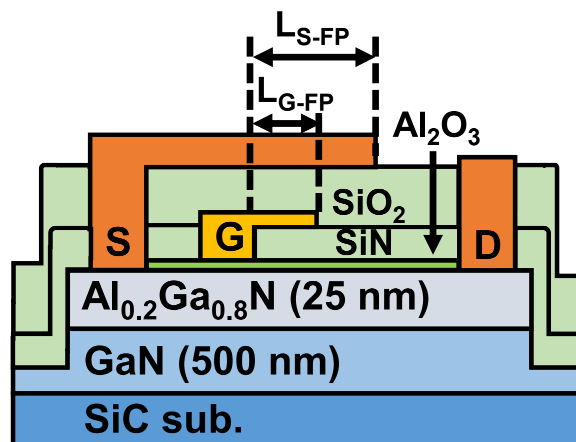

Fig. 1. Cross-sectional view of dual-FP MOS-HEMT.

The device process started with mesa-isolation using ICP reactive ion etching (RIE) by BCl_3/Cl_2 mixed gases. Source/drain ohmic metallization was made by evaporating Ti/Al/Mo/Au (15/60/35/50 nm), followed by annealing at 850 °C for 30 s. Then, Al_2O_3 (10 nm) was deposited by atomic layer deposition (ALD) at 250 °C. Ni/Au (50/150 nm) was deposited as a gate electrode. Devices were then passivated with a 150 nm sputter-deposited SiN film. The gate window was opened by dry etching of the SiN film and then Ti/Au (10/200 nm) was deposited to form G-FP. After depositing 400 nm-thick SiO_2 film, Ti/Au (10/200 nm) was deposited to form S-FP. Devices with no FPs were also fabricated for comparison.

CURRENT COLLAPSE MEASUREMENT

Fig. 2 shows the measurement setup of the current collapse. A drain bias was supplied in series with a load resistance (R_L), while a train of gate pulses was applied to the gate. The dynamic on-resistance (R_{on}) was directly evaluated within the linear region of the device I-V characteristics. The on-state and off-state duration times for the gate pulse were 1 μs and 10 ms, respectively. As a measure of current collapse, the normalized dynamic on-

resistance (NDR) was defined by the measured dynamic R_{on} divided by the value of static R_{on}.

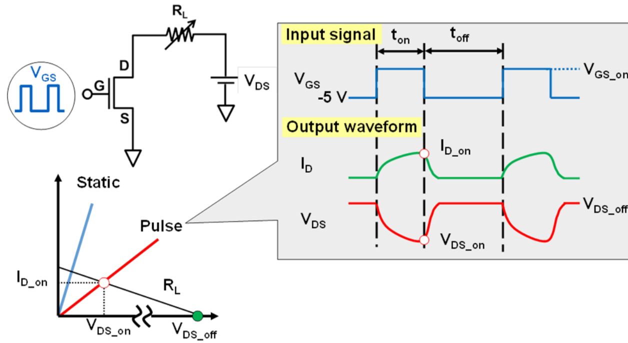

Fig. 2. Measurement setup of current collapse.

RESULTS AND DISCUSSION

Fig. 3 shows drain output and transfer characteristics of the fabricated AlGaN/GaN dual-FP MOS-HEMT. The device exhibited a maximum drain current of 0.7 A/mm with a threshold voltage of -4.5 V. Furthermore an excellent on/off current ratio of more than 10^7 was achieved with a subthreshold swing of 88 mV/dec.

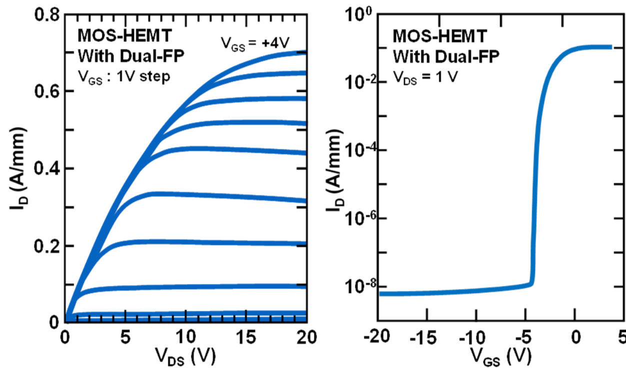

Fig. 3. Output and transfer curves of dual-FP MOS-HEMT.

Fig. 4 plots the normalized dynamic R_{on} (NDR) as a function of the off-state drain voltage (V_{ds_off}) for devices with and without FPs. Note that the degradation in NDR was almost perfectly suppressed for the dual-FP MOS-HEMT up to V_{ds_off} of 100 V, while the NDR degradation was appreciably observed for the conventional device with no FPs and the device with only S-FP. Fig. 5 shows the measured NDR as a function of gate-to-source voltage (V_{gs}) during on-state. In the negative V_{gs} region, the difference in NDR was negligible between devices with S-FP and G-FP. However, applying more positive V_{gs} values resulted in significant reduction in the current collapse for the G-FP device. At V_{gs} = +3V, the G-FP device exhibited 10 times more improved NDR as compared to the device with only S-FP. The superior performance in current collapse by using G-FP is well explained by the fact that an additional channel

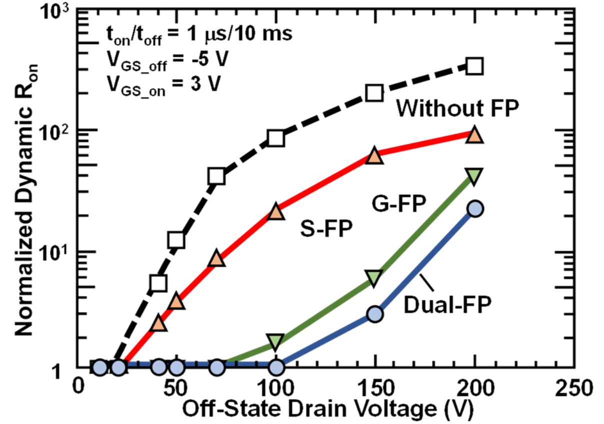

Fig. 4. NDR as a function of off-state drain voltage.

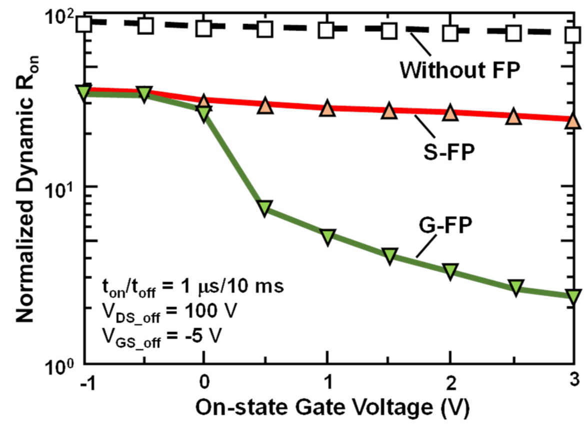

Fig. 5. NDR as a function of gate-to-source voltage.

charge is instantly generated under the G-FP region during the gate voltage maintained more than 0 V. The capacitively generated additional channel charge during on-state is effective to compensate the depletion of 2-dimensional channel electrons, resulting in reduced dynamic on-resistance characteristics. This is the main reason why we observed more enhanced improvements in current collapse only for the G-FP device, as has been shown in Fig. 5.

The forward gate bias step-stress measurements were performed with V_{gs} values sweeping from +1 to +5 V with a step of 1 V. Each step stress was maintained for 10 min. After each stress step, I_d-V_{gs} transfer characteristics were measured at V_{ds} = 1 V to monitor any changes in V_{th} and gate leakage current. As shown in Fig. 6, no such changes in V_{th} was observed up to the forward gate stress of +4 V, while a sudden increase in the gate leakage current by 4 orders of magnitude was observed with a gate stress voltage of +5 V. A slight increase in V_{th} was also observed with increasing the forward gate stress voltage. The positive V_{th} shift after bias stress at V_{gs} = +4 V was less than 0.3 V.

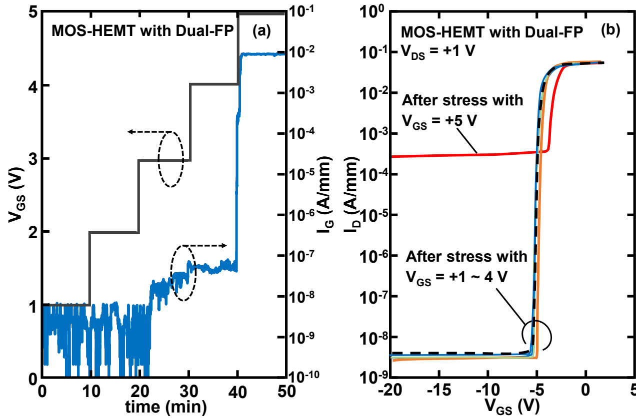

Fig. 6. Forward gate stress waveform (a), and transfer curves (b).

Figure 7(a) shows the time schedule for the reverse gate bias step-stress measurements conducted with a gate-to-drain voltage (V_{gd}) sweeping from -100 to -600 V with a step of 100 V. The results for the reverse gate-stress testing were displayed in Figs. (b), (c) and (d) for the MOS-HEMTs without FPs, with G-FP, and with dual FPs, respectively. No V_{th} shifts were observed after reverse step-stress measurements for all the MOS-HEMTs tested. However, a significant degradation in the drain current was verified for the MOS-HEMT without FPs after a reverse gate stress more than 100 V, as shown in Fig. 7(b). Meanwhile, such drain current degradations were hardly observed for MOS-HEMTs

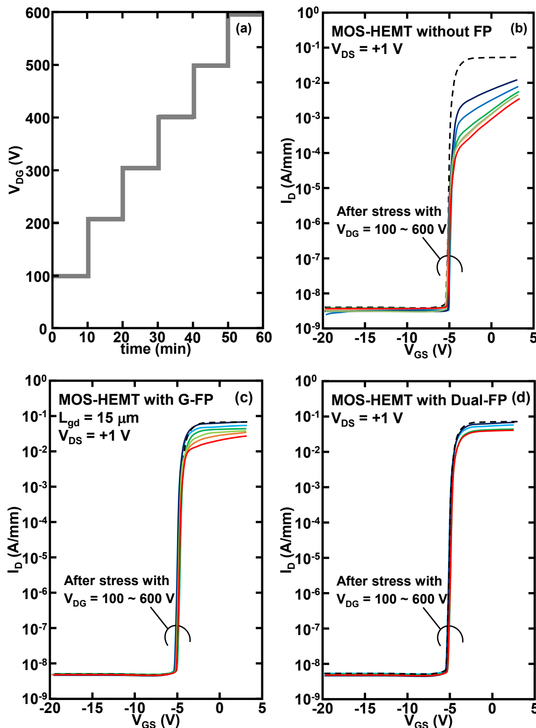

Fig. 7. Reverse gate stress waveform (a), and transfer curves for without FP (b), with G-FP (c), with dual-FP (d).

with G-FP and dual-FPs. In particular, the dual-FP device exhibited negligible degradation in the drain current even after a stress bias of -600 V, as shown in Fig. 7(d). These results suggest that the electric field concentration at the gate edge in the drain side was relaxed by using G-FP. The dual-FP device is more beneficial for suppressing the drain current degradation since the electric field concentration at the edge of G-FP was further reduced by the S-FP. As a result, the dual-FP device demonstrated the best performance in suppressing current collapse and degradation by negative gate bias stressing.

To show the feasibility of high-voltage and high-current operation of the developed dual-FP MOS-HEMT, we have fabricated a multi-finger device with a total gate with of 54 mm. Figure 8 shows a SEM image of the multi-finger device developed for enabling flip-chip bonding with a chip size of 3 mm x 3 mm. The device exhibited a maximum drain current of 21 A with an off-state breakdown voltage of 950 V (see Figs. 9 and 10). To avoid any undesirable field crowding at the drain electrode edge, we have used a newly-designed electrode pattern, in which the corners of the drain electrode were rounded [6].

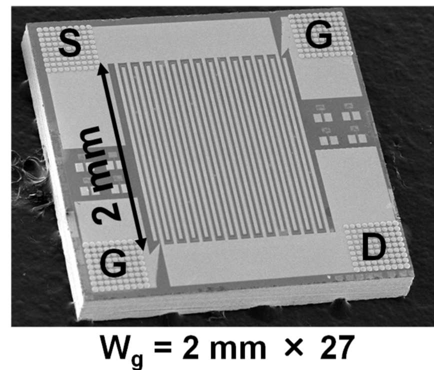

Fig. 8. SEM image of MOS-HEMT with W_g = 54 mm.

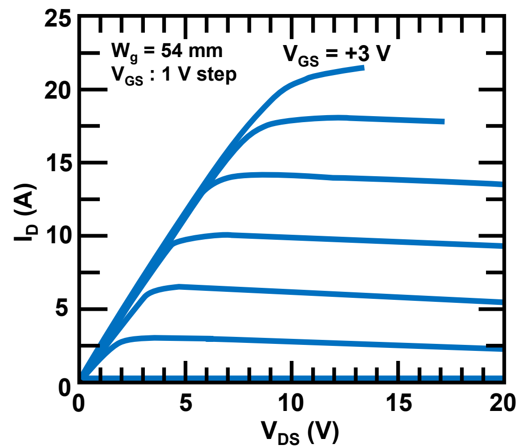

Fig. 9. Drain I-V characteristics of dual-FP MOS-HEMT with W_g = 54mm.

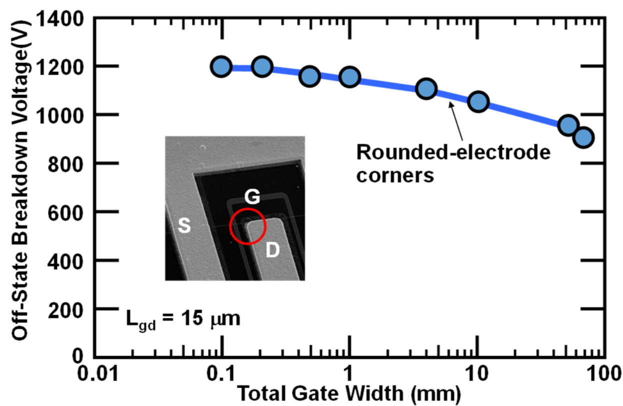

Fig. 10. Off-state breakdown voltage as a function of total gate width.

Conclusions

We have developed an AlGaN/GaN MOS-HEMT with both gate and source FPs to ensure best performance in DC and dynamic on-resistance characteristics. In addition, the dual-FP device exhibited excellent stability after positive and negative gate bias step-stress measurements. Finally, a large gate width MOS-HEMT delivered a maximum drain current of 21 A with an off-state breakdown voltage of 950 V.

Acknowledgements

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Acronyms

HEMT: High Electron Mobility Transistor
MOS: Metal Oxide Semiconductor
ALD: Atomic Layer Deposition
FP: Field Plate
NDR: Normalized Dynamic On-Resistance
W_g: Gate width