Towards a Si Foundry-Compatible, High-Performance, ≤0.25 µm Gate, GaN-on-Si MMIC Process on High-Resistivity 200 mm <111> Si With A Cu Damascene BEOL

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Abstract

Raytheon is developing a 200 mm GaN on Si MMIC process suitable for standalone high frequency MMIC applications, and for heterogeneous integration with Si CMOS, SiGe BiCMOS and other III-Vs. Building on previous 100 mm and 200 mm GaN-on-Si work [1-5], this work reports progress towards a fully integrated MMIC, as well as the world's first X-Band GaN 0.25 µm power transistor on 200 mm diameter Si wafers. This GaN-on-Si HEMT delivers 4.7 W/mm with 9 dB gain with 49% PAE at V_d = 28 V. The wafers were fabricated at Novati Technologies, a commercial CMOS foundry, using a fully subtractive, Au-free, Si-like fabrication approach.

INTRODUCTION

Over the last decade, gallium nitride (GaN) has garnered considerable interest for use in power electronics and high power density and high-linearity RF applications. It is clear that the large commercial volume for 200 mm GaN on Si wafers will be driven by power electronics applications. As these applications begin to fill 200 mm foundries, however, high-performance GaN-on-Si RF MMIC applications will naturally follow and take advantage of the large-diameter wafers and background wafer volume to reduce cost for RF ICs.

Beyond the cost advantage for GaN on Si MMICs fabricated on 200 mm wafers, large-diameter wafer fabrication offers advantages for heterogeneous integration of GaN HEMTs with silicon CMOS (for additional functionality) when compared to a die-to-wafer approach. While compatible with die-to-wafer integration, wafer-to-wafer heterogeneous integration of 200 mm GaN ICs with 200 mm CMOS is more promising in terms of shorter interconnect lengths and improved yield for high-density, high-performance ICs.

To facilitate these future cost, yield, and functionality improvements, Raytheon is developing a submicron (≤0.25 µm gate) GaN-on-Si MMIC process on high- resistivity 200 mm <111> Si with a Cu damascene BEOL process. The key aspects of this process are:

- fabrication in a 200 mm Si foundry
- fully subtractive (no liftoff) Au-free process
- fabrication on high-resistivity wafers with low breakage
- 200 mm GaN-on-Si epitaxy by both MBE (in-house) and MOCVD (IQE)
- multilevel Cu damascene-based back–end-of-line (BEOL) process
- integrated passive elements
- Cu metal integrated into gate structure
- all optical ≤0.25 µm gate process
- low-temperature Au-free Ohmic contacts

This work reports progress towards a fully integrated MMIC as well as the world's first Si foundry-compatible X-Band GaN 0.25µm power transistor on 200 mm diameter Si wafers.

RESULTS AND DISCUSSION

MOCVD and MBE GaN-on-Si epitaxy is grown on high resistivity, SEMI-standard thickness (725 µm) 200 mm diameter wafers, and display ≤50 µm wafer bow with excellent electron mobility (~1,600 $cm^2/V{\cdot}s$).

The low wafer-bow, SEMI-standard thick wafers enable the use of production-level, 248 nm and 193 nm scanner lithography systems in our front-end-of-line (FEOL) transistor process. This in turn enables tight layer-to-layer alignment tolerances for the submicron gate in our FEOL. The use of low-temperature (≤ 600ºC) Ohmic contacts in our FEOL improves Ohmic contact morphology, which facilitates back-end-of-line (BEOL) interconnect processes.

These processes have been used to demonstrate 0.25 um gate, X-band (10 GHz) GaN-on-Si HEMTs on 200 mm wafer grown by MBE (Fig. 1). These devices, processed fully subtractively, deliver 3.6 – 4.7 W/mm with 7-9 dB gain and 48-49% PAE at V_d = 20-28 V, respectively. Results are expected to improve as the process matures.

The multi-level Cu damascene BEOL process has been optimized for high current density. We have successfully integrated SiNx MIM capacitors and tantalum nitride (TaN) thin-film resistors into our Cu BEOL process (Figs. 2-4).

More recently, we began developing a backside via fabrication process to facilitate microstrip MMIC fabrication on 200 mm GaN-on-Si wafers thinned to 50 µm. Raytheon has scaled its 100 mm backside wafer mounting and thinning process to 200 mm for this purpose. As shown in figure 5, a standard Si foundry Bosch etch process is used to etch the via through the Si substrate. A second chlorine-based etch completes the via by etching the remaining GaN HEMT layers.

All the key process modules have been developed for 200 mm GaN-on-Si MMIC fabrication. Process integration and optimization are continuing and being used to fabricate GaN-on-Si RF ICs.

CONCLUSION

To our knowledge, this is the first report of X-Band performance using 0.25 µm gate GaN HEMTs fabricated in a 200 mm Si foundry fabricated with a Cu BEOL within the context of a microstrip MMIC process.

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ACRONYMS

BEOL: Back End of Line
BiCMOS: Bipolar/Complementary MOS
CMOS: Complementary Metal Oxide Semiconductor
CW: Continuous Wave
FEOL: Front End of Line
HEMT: High Electron Mobility Transistor
ICs: Integrated Circuits
MBE: Molecular Beam Epitaxy
MIM: Metal-Insulator-Metal
MMIC: Monolithic Microwave Integrated Circuit
MOCVD: Metal Organic Chemical Vapor Deposition
PAE: Power-Added Efficiency

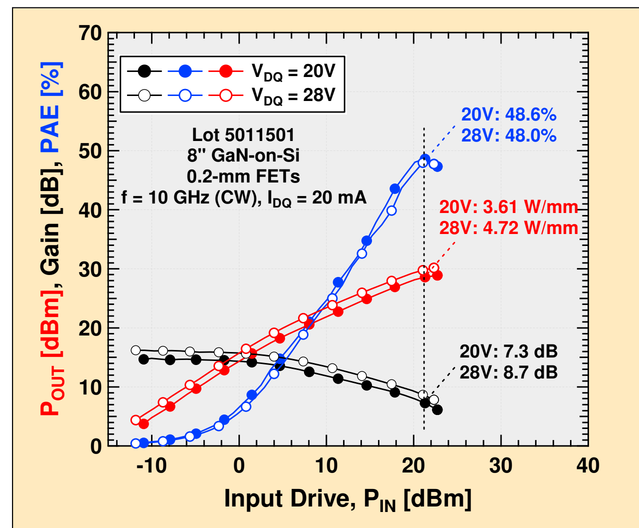


Fig. 1. 200mm X-Band (10 GHz) MBE GaN-on-Si HEMT delivers 3.6 – 4.7 W/mm with 7-9 dB gain with 48-49% PAE at 20-28 V

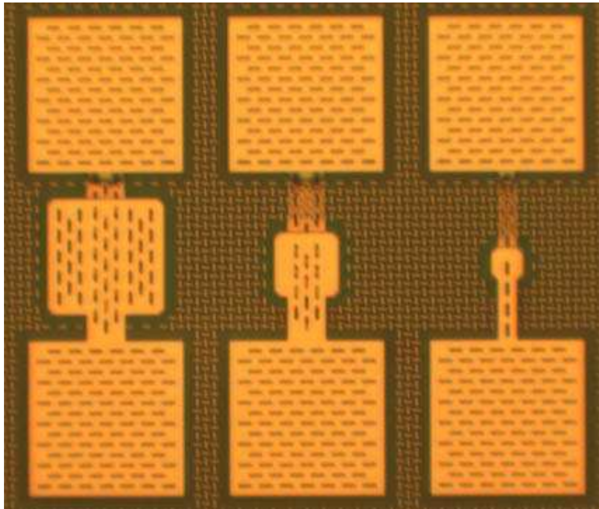
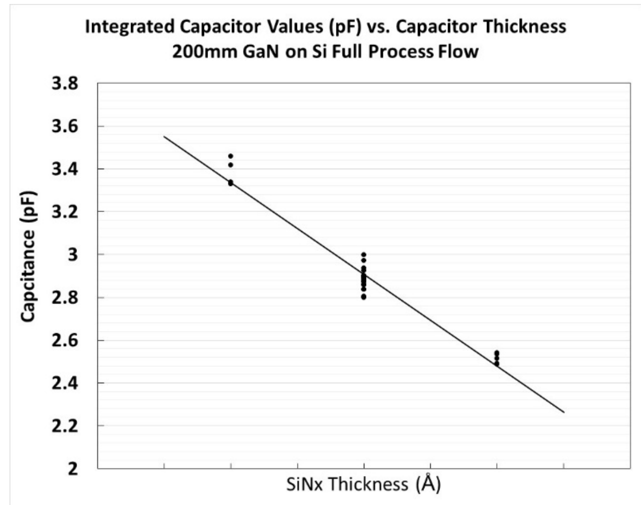


Fig. 2. Process Control Monitor (PCM) Capacitors integrated into Cu Damascene BEOL



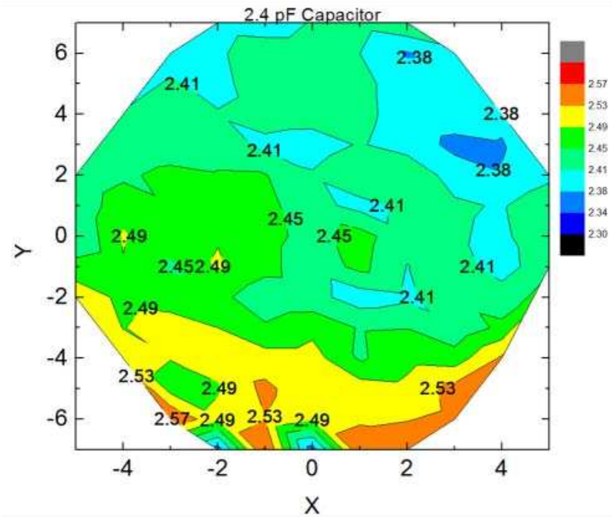
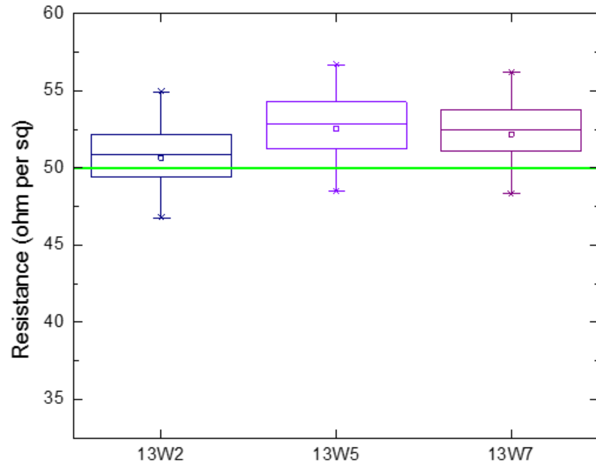


Fig. 3. SiNx Capacitor tuning experiments on 200mm GaN on Si HEMT with a Cu Damascene BEOL (Top). Wafer map of integrated capacitors within a Cu Damascene BEOL with tight distribution of capacitance values (Bottom).



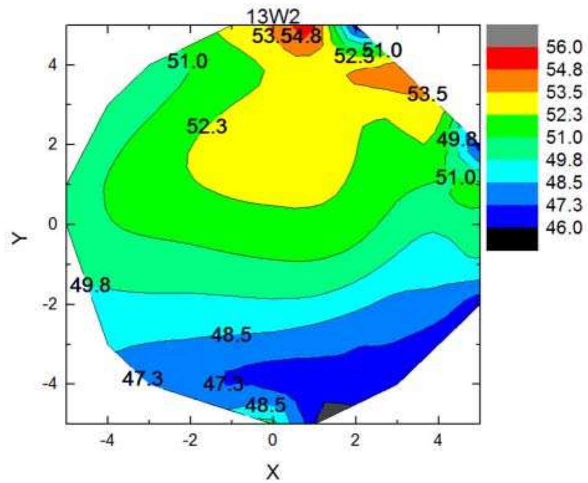


Fig. 4. Box plots of TaN resistor sheet resistance optimized to 50 ohm/square as measured on cross bridge structures on 200mm GaN on Si wafers with a Cu BEOL (Top). TaN sheet resistance map from wafer #2 of box plots with tight distribution of sheet resistance values (Bottom).

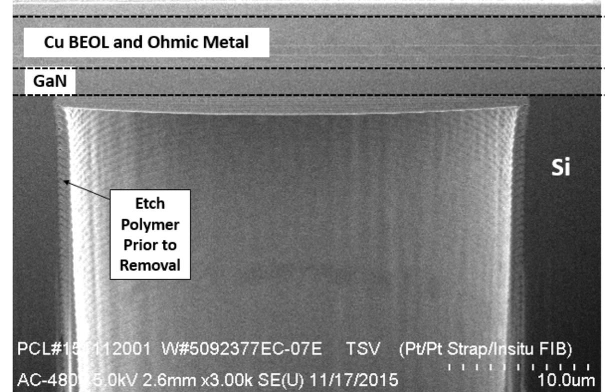


Fig. 5. Partially completed GaN HEMT backside via etch. The through substrate via (TSV) is etched through the thinned 50µm Si substrate using a standard BOSCH etch which stops selectively at the GaN HEMT nucleation layer. The via etch is completed with a chlorine based etch to remove the GaN layer.