Challenges for Establishing a High Volume, High Yielding BiHEMT Manufacturing Process

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Abstract

In this paper, we report the development of a BiHEMT process, the integration of InGaP/GaAs heterojunction bipolar transistor (HBT) with pseudomorphic high electron mobility transistor (pHEMT), and the process challenges for establishing a high volume, high yielding, and commercially manufacturable BiHEMT process. The integration of HBT and pHEMT gives the designers additional freedoms for the design of advanced bias, logic, RF switch, low noise figure amplifier, and circuit functionality. Since pHEMT is integrated underneath the HBT sub-collector layer, severe topology issues are introduced. Therefore, process challenges related to this severe topology must be solved in order to obtain a high volume, high yielding, and manufacturable process.

INTRODUCTION

InGaP/GaAs heterojunction bipolar transistors (HBTs) have become the dominant transistor technology for wireless handset power amplifier (PA) applications due to their excellent RF performance, reproducibility, and manufacturability. To increase design flexibility, circuit functionality, reduce module size and overall module cost, MESFET or pHEMT devices have been successfully integrated with HBTs on the same chip [1-5].

In this paper, we will discuss the fabrication challenges and yield improvement activities during the process development of a high yield BiHEMT technology established for Skyworks products. Epi structure and device fabrication are briefly addressed. Due to severe topology introduced in the BiHEMT process, many process challenges, such as pHEMT gate finger missing, emitter shorting due to resist erosion of TaN film resistor and inter-level metal shorting were observed, which are discussed in this paper. Moreover, fabricated HBT performance and yield results are presented.

EPI STRUCTURE AND DEVICE FABRICATION

BiHEMT technology utilizes MOCVD-grown epitaxial material with Skyworks HBT epitaxial structure on top of the pHEMT epitaxial layers. First, pHEMT epitaxial layers are grown on 150 mm semi-isolating GaAs substrate. To optimize the pHEMT performance and meet the requirements for high volume production, each layer of the pHEMT is finely tuned and there is no layer that is shared with the layer of the HBT devices. After the pHEMT layers are grown, the HBT sub-collector layer and the following collector, base, and emitter epitaxial layers are grown subsequently. Slight modifications of the Skyworks original HBT layer stack have been performed to accommodate the implementation of the pHEMT device underneath the HBT structure. To minimize the possible degradation of pHEMT device performance, special care needs to be taken during HBT layer growth, and etch stop layers need to be inserted for process robustness.

BiHEMT fabrication steps start with emitter contact formation, which utilizes metal evaporation and liftoff. The emitter mesa is formed by ICP dry etch, which stops on top of the InGaP HBT emitter layer. The base pedestal is defined also by ICP dry etch. A PECVD silicon nitride film is deposited to protect the HBT active area. To access the pHEMT layers, a sub-collector layer is wet etched. Base contact is formed by silicon nitride etch, InGaP layer etch, metal deposition and liftoff. Collector contact is defined by AuGeNi/Au metal system deposition and RTP alloy process. The pHEMT source and drain ohmic contact is formed simultaneously with the HBT collector. He+ implantation is used to electrically isolate devices, diodes, and other passive components. The pHEMT gate is defined by photo lithography, gate recess wet etch, Ti/Pt/Au gate metal deposition and liftoff. After the intrinsic HBT and pHEMT are formed, PECVD silicon nitride film is deposited for devices passivation. The following process modules include TaN thin film resistors, MIM silicon nitride capacitors, inductors and metal interconnections. The BiHEMT front side process is completed with final passivation silicon nitride deposition.

PROCESS CHALLENGES

Compared to the standard HBT process, the process challenges for the BiHEMT process mostly arise from the severe topology created by active devices, passive components, metal interconnections, and dielectric layers. The step height from the top of the HBT emitter contact to

the pHEMT gate layer at the bottom is roughly 2 µm, as show in Fig. 1.

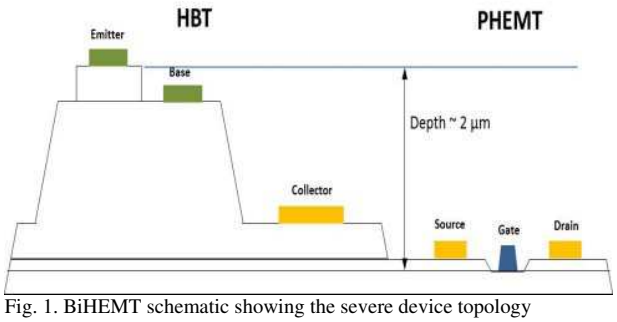

Fig. 1. BiHEMT schematic showing the severe device topology

In BiHEMT structure, the pHEMT gate is sitting underneath HBT sub-collector on the bottom level of topology. With ~2 µm depth topology, to open and etch the pHEMT gate Schottky layer with good uniformity and process control, photo and etch process optimization for the gate formation are critical. In a high volume production environment, any process issue and/or narrow process margin can cause disastrous wafer scrap, cost increase and yield loss. In our BiHEMT production practice, we found that an unoptimized gate photo process often leads to missing gate metal, as depicted in Fig. 2. To understand and monitor the degree of the missing gate issue, a novel method to pre-screen the gate yield was developed and implemented at the post gate metal formation step, before the completion of the process and the PCM test. Fig. 3 (a) shows the missing gate percentage before process optimization.

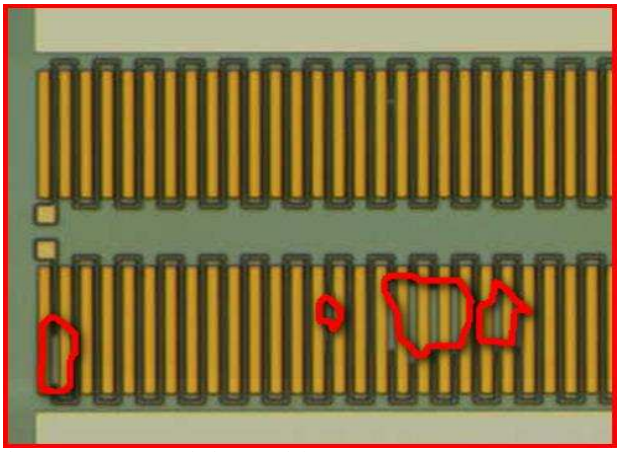
Fig. 2. pHEMT gate missing at reticle corner

Before the gate photo was optimized, the yield loss could be as high as about 20%. By optimizing specific gate photo exposure conditions, equipment tuning and mask modification, we were able to eliminate the missing gate issue and improved the gate integrity yields up to 99%, as shown in Fig. 3 (b).

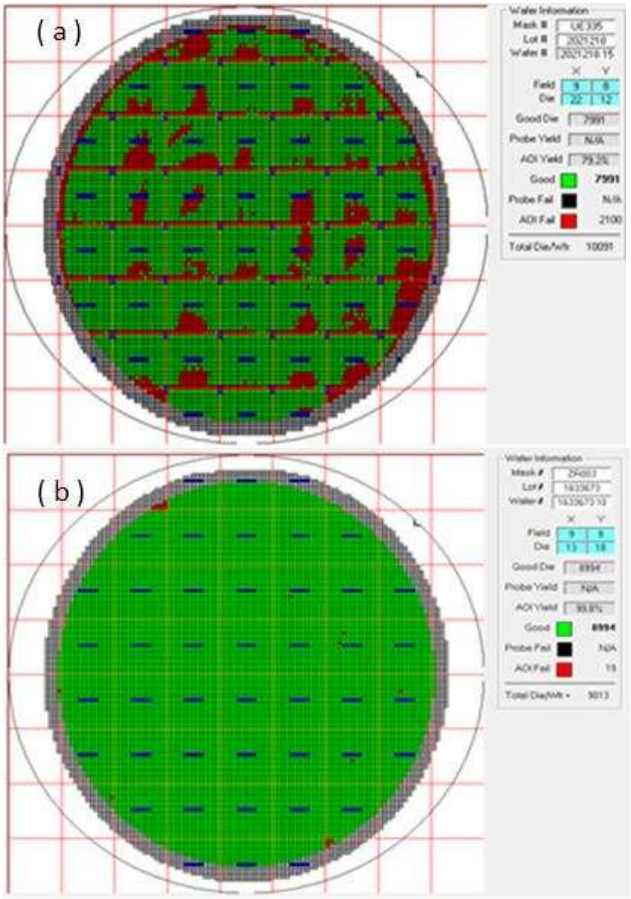

Fig. 3. (a) Gate integrity yield loss due to missing gates was typically seen at reticle field corners and (b) Optimized process gate integrity yield

Another process challenge for high volume high yield BiHEMT process is the photoresist erosion observed in the thin film TaN resistor process, which is also a topology-related process issue. The TaN resistor, located at the pHEMT level, requires dry etch of silicon nitride before the TaN deposition to achieve a clean lift-off (Dielectric Etch Assisted Lift-off). Due to the photo resist not being perfectly conformal, the resist thickness on top of the HBT emitter is much thinner than that on the TaN level, as shown in Fig. 4 (a). The resist thickness on top of the HBT emitter could be less than 1000 Å. During the TaN resistor silicon nitride dry etch process step, the photoresist on top of the HBT emitter was fully eroded, resulting in TaN metal deposition on top of the HBT emitter. This in turn prevents the HBT Metal-1 metal connecting to emitter metal and/or results in emitter short and yield loss, as shown in Fig. 4 (b). The yield loss typically introduced by the issue of TaN deposited on the emitter is about 3% at final probe test.

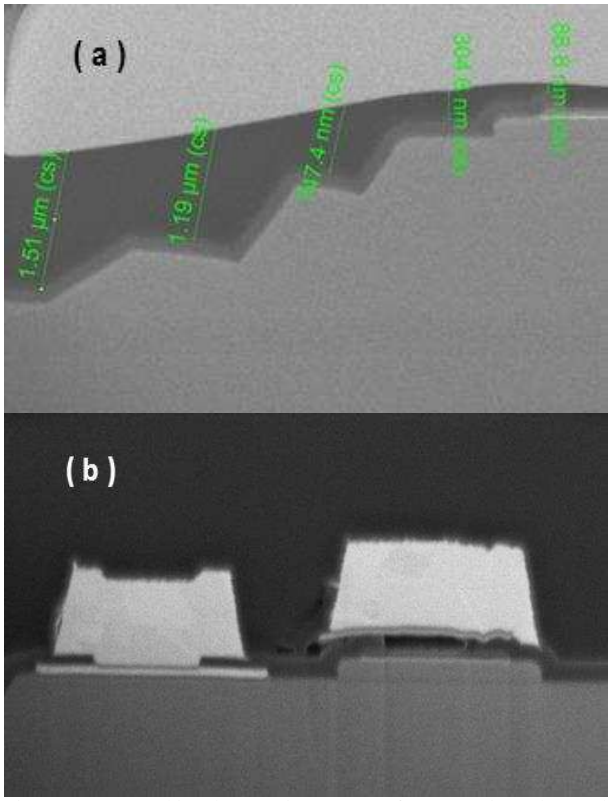

Fig. 4. (a) Very thin photo resist on top of HBT emitter due to high topology and (b) TaN metal deposited on top of HBT emitter, preventing the M1 from connecting the emitter

There are two methods to eliminate unwanted TaN metal on top of the HBT emitter. The first method is simply by increasing the resist thickness at this step. However, since the resist was not very conformal, simply increasing the resist thickness did not significantly improve resist coverage on top of the emitter. In fact, increasing the resist thickness on the TaN resistor level makes TaN resistor CD control more difficult, and hence impacts probe test yield. The second method is combination of selecting a more conformal photo resist to improve the resist coverage, and moderately increasing the resist thickness. In our practice, we have selected the second method for TaN resist process, which resulted in the recovery of this yield loss, without impacting the electrical performance.

In addition to introducing device processing step challenges, severe BiHEMT topology also impacts some of the backend of line process modules, leading to inter-level metal interconnection shorts and/or poor isolation. Fig. 5 shows Metal-2 metal shorts to Metal-3 metal at severe topology areas. Due to the severe underlying topology, photo resist and inter-level dielectric (ILD) material coverage are poor. At subsequent ILD dry etch step, the resist and even dielectric material get etched away, resulting in short between the interconnection metals. Additionally, the presence of metal stringers will further increase the yield loss. The failure impact of this metal short is fatal. The yield loss is typically large and can result in wafer scrap.

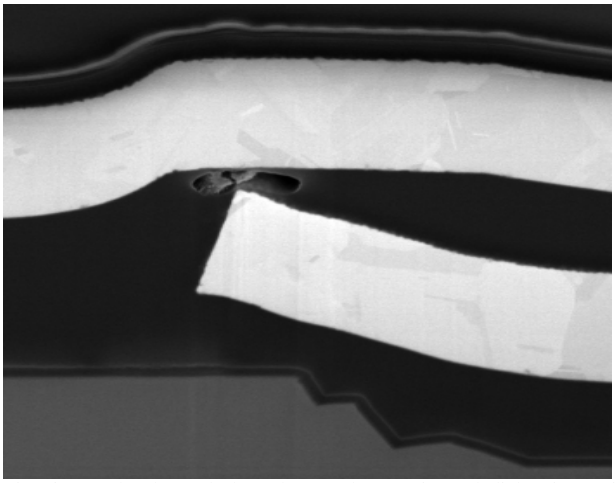

Fig. 5. Inter-level metal short due to photo resist and dielectric erosion during dry etch

Multiple process steps are taken to solve the inter-level metal short issue. One step is simply increasing the photo resist thickness to increase the process margin. However, due to the photo resist conformability issue, the resist thickness on top of the topology does not increase sufficiently. The second step is process condition optimization at inter-level dielectric layer dry etch step. This process optimization involves improving the etch ratio of dielectric to photo resist leading to elimination of the erosion of the protected dielectric area. The third step is to optimize inter-level metal stacks. With above optimizations, we have eliminated the inter-level metal short and improved the probe yield by about 3.8%. Fig. 6 shows the inter-level dielectric thickness comparison before and after process optimization.

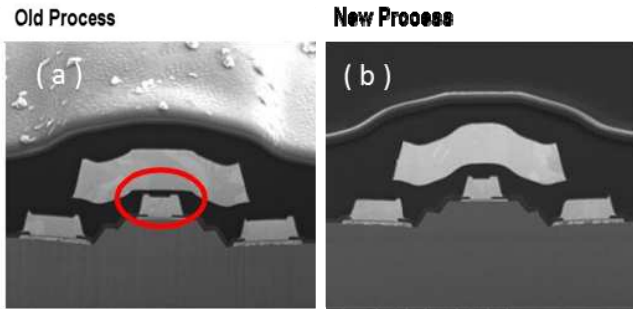

Fig. 6. Dielectric erosion improvement comparison. (a) Before process optimization and (b) Post process optimization

RESULTS

The DC and RF parameters of the fabricated BiHEMT wafers have been characterized and the results show that the

HBT performance is comparable to that of our HBT-only technology, and the pHEMTs provide the required RF performance for various circuit applications.

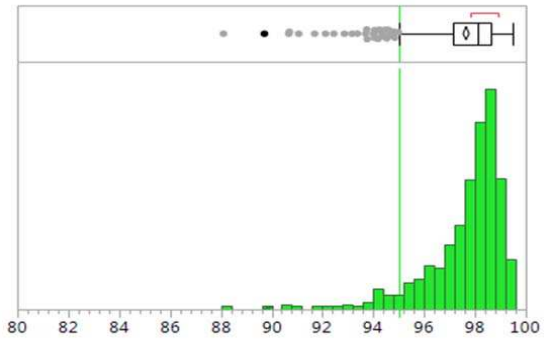

Fig. 7. Die-sort yield of a representative BiHEMT mask

Realizing high yield in BiHEMT technology not only depends on the optimization of multiple process modules, but also critically relies on the testability and test coverage in die-sort. After resolving all the topology-related process issues, probe die-sort yield in BiHEMT technology is consistently running over 95%, as shown in Fig. 7.

CONCLUSIONS

A BiHEMT technology, the integration of InGaP/GaAs HBT and pHEMT, has been successfully developed and released to Skyworks high volume production line. Process issues which impacted final probe test yields, such as gate metal missing, TaN metal deposition in the emitter due to resist erosion, inter-level metal short caused by dielectric erosion, have all been resolved. Together with process margin improvements, a high yielding BiHEMT process has been achieved.

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ACRONYMS

PA: Power Amplifier
HBT: Heterojunction Bipolar transistor
PHEMT: Pseudomorphic High Electron Mobility Transistor
BiHEMT: Monolithically Integrated Bipolar HBT and PHEMT
TaN: Tantalum Nitride thin film