

Reducing Power vs. Time (PvT) Failure in BiFET2 Device Technology

Sajid H. Shamsi

Sr. Device Engineer (Yield/Quality), Qorvo, Inc, 7628 Thorndike Rd, Greensboro, NC 27409

e-mail: Sajid.Shamsi@Qorvo.com, Phone: (336)-402-3711

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Abstract

Integrated circuits used in Qorvo's BiFET2 technology are composed of Heterojunction Bipolar Transistors (HBT) and pseudomorphic High Electron Mobility Transistors (pHEMT) on a single (GaAs) substrate. (pHEMT) is also referred to as (FET) field effect transistor. These circuits are composed of logic and power amplifier applications utilizing FETs and HBTs respectively. It has been observed, that in order to achieve the intended application from these devices, FET and HBT parameters need to be fully optimized. Any degradation in device characteristic will result in degraded performance. One such failure is (PvT) Power vs Time which is significantly dependent on FET switching capability. If FET devices do not perform as intended, (PvT) failure could occur in module yield loss. Optimizing FET to reduce (PvT) failure will be the focus of this paper.

INTRODUCTION

Optimizing FET performance for switching application in a circuit requires all critical device parameters to be fully optimized to achieve the desired results [1]. One of the main aspects of this application is to reduce and eliminate any transient time when switching among different power modes. This requires FET to operate in linear region of the device to achieve high drive current (I_{ds}), high transconductance (G_m) and low ON resistance (R_{on}) at the desired pinch-off voltage (V_{po}). These parameters are mainly affected due to variations in Epi. Since FETs in this application are used to bias 1st, 2nd and 3rd stages of power amplifiers (PA), optimizing these parameters through Epi can significantly improve switching capability resulting in higher (PA) current gain. If these critical FET parameters are not controlled to achieve the intended targets, it can result in product yield loss by failing one of the product test parameters called (Settling_Delta) discussed further in the proceeding section. In addition to Epi variation in FET parameters, circuit design marginalities and thermal component are also contributing factors in degrading

PA performance. Since the thermal component contributing to this failure will require new design changes, the focus of this paper will be on optimizing FET performance and biasing capability through Epi process improvements. In a production environment, this approach is more cost effective and manageable resulting in increased product performance which helps enhance module yields.

GaAs (FET) EPI STRUCTURE

Understanding Epi structure for high performing (pHEMT) is very important. A typical AlGaAs structure with InGaAs channel is composed of the following Epi layers Structure as shown in Table 1.

Table-1: FET Epi Layer Structure

Layer	Layer Name	Material	Type
1	GaAs Contact	GaAs	N+
2	Schottky	AlGaAs	N
3	Upper Charge	AlGaAs	N+
4	Upper Spacer	AlGaAs	UnD
5	Channel	InGaAs	UnD
6	Lower Spacer	AlGaAs	UnD
7	Lower Charge	AlGaAs	N+
8	Superlattice	AlGaAs/GaAs	UnD
9	Buffer	GaAs	UnD
10	Substrate	GaAs	Si

In order to produce high performing (GaAs) FET devices, channel charge, thickness and AlGaAs composition of all layers in Epi structure should be optimized to obtain these required target values of critical FET parameters. One such aspect of FET switching application is to obtain the highest level of drive current I_{ds} required by a circuit design. Fig (1) shows an example of I_{ds} response to $|V_{pol}|$ with respect to G_m .

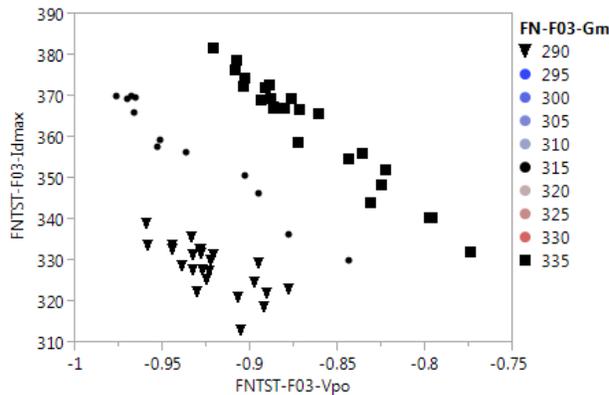


Fig.1. Correlation of Ids vs Vpo (w.r.t) Gm.

Above data shows a response of Ids with respect to Gm ranging from Low-to-High values. The above plot also shows that by increasing Gm, we can produce higher Ids for required Vpo target. This is critical to any GaAs (FET) affective switching application. Transfer curves for respective FET with high and low Gm wafers are shown in Fig.2. These electrical characteristic curves confirms that Gm is decreased by a certain magnitude at the max point when Vgs=0 and where Ids is transitioning in to saturation region.

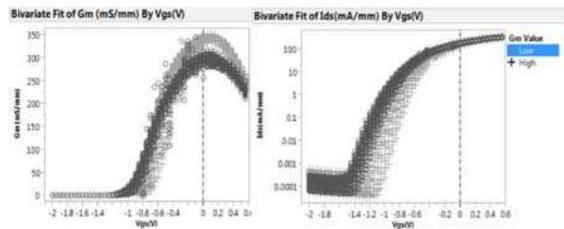


Fig.2. Transfer curves with respect to Gm.

Before we look at the circuit design optimization for reducing (PvT) failures, we first need to analyze interactions and dependency of each Epi layer to achieve the desired Gm and Vpo. What we have learned from our experiment and in production environment, is that Gm and Vpo can be optimized, reproduced and controlled by improving critical layers in Epi structure. For better Gm control with minimum variability, composition of Alloys in (AlGaAs) for upper and lower charge layer should be optimized. In addition to that, the spacer layer thickness should also be optimized to be able to achieve the desired Gm target. On the other hand, for better Vpo control, (Ns) channel charge doping and Schottky thickness should be optimized. Once we adjust the correct AlGaAs composition, doping and thickness for the above mentioned layers, we can achieve the highest Ids resulting in faster switching

speed with zero transient time. For BiFET2 technology, Epi is grown with the MOCVD process. The tradeoff of using this process is the layer thickness uniformity across wafer [3]. This thickness variation can cause |Vpol variation across wafer. For FET to stay in linear region of operation, this thickness needs to be tightly controlled with good standard deviation.

POWER vs TIME

Power vs Time failure is define as the ability of an Amplifier to maintain a specified output power over a specified time interval when switching from different power modes. Test at the product level which tracks (PvT) failures is called (Settling_Delta) which measures time delta of power gain stability among different power modes. For example, the failure occurs when it takes a longer time for low power gain to get stable after switching from High Power Mode to Low Power Mode (HPM-to-LPM). Figure 3 shows an example of (PvT) fail with respect to Settling_Delta distribution.

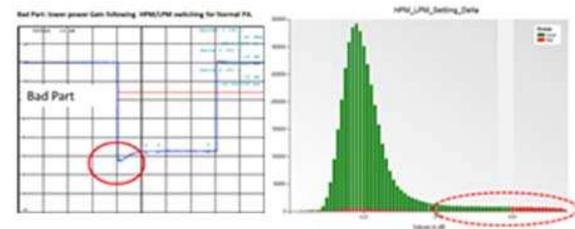


Fig. 3. PvT Problem showing where power level does not recover to steady state for an extended Period of time.

Since FETs are used in biasing different stages of (HBT) PAs, any Ids current degradation can cause PvT and ILPC test failures. ILPC is define as an inner loop power control test which measure the transmit power at each switching point. The goal is to reduce or eliminate this variability and to produce all parts within the 3-sigma distribution range of (Settling_Delta). Following is an example of an ILPC comparison showing good and bad profile of the low power gain following switching from (HPM-to-LPM). Referenced in Fig.4. From the figure below, curve (a) shows a normal case when the PA low gain has already been stable while doing ILPC test. On the hand, curve (b) indicates an abnormally long time duration to get stable resulting in different gain values in ILPC test.

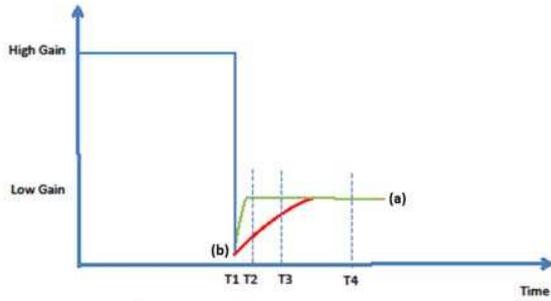


Figure 1
Fig.4. (a) Stable low power gain following (HPM-to-LPM) switching for normal PA part. (b) The low power gain following (HPM-to-LPM) switching for a defective PA part.

T1- Switching point time when PA starts to switch.
 T2-Start time to measure the transmit power in the first slot following the switching point in ILPC test.
 T3- Start time to measure the transmit power in the second slot following the switching point in ILPC test.
 T4-Time to measure the transmit power of the low power gain in calibration process.
 Further results for corresponding Passing and Failing are shown in Fig.5.

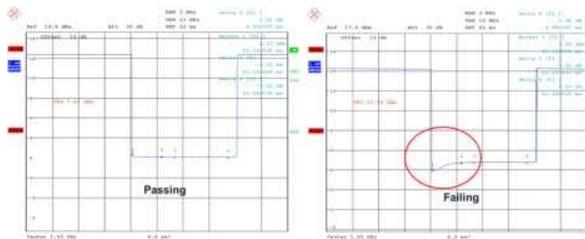


Fig.5. PvT Issue for “Passing vs. Failing”

DEPLETION MODE FET RESPONSE IN A CIRCUIT

This explanation is based on using an Attenuator circuit to reduce P_{out} for LPM power mode. There are several circuit design improvements that could be incorporated to reduce P_{out} when switching from high to low power modes however here we will discuss the V_{po} approach to achieve this objective. Consider the following example of an Attenuator circuit that uses three D-mode (Depletion mode) FETs. This circuit configuration is shown in Fig.6.

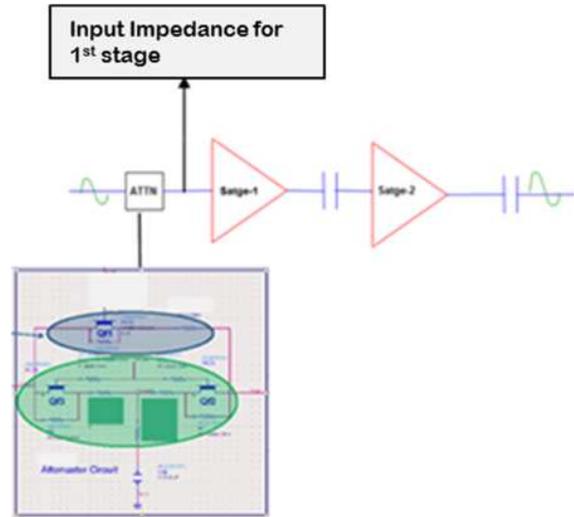


Fig.6. Depletion mode FETs in the circuit.

The intended operation for LPM is accomplished by having Qf1 “pinched off” enough to allow sufficient I_{ds} current to discharge the attenuator’s input and output impedances. Qf2/Qf3 are left fully turned ON providing only negligible series open channel resistance (R_{on}). Problem occurs, when Qf1 pinch off voltage magnitude ($|V_{pol}|$) is too small. Since, we are sweeping V_{gs} with negative bias voltage towards ($V_{gs}=0$), $|V_{pol}|$ will decrease and I_{ds} will start to shift in saturation region causing G_m to decrease as well [4]. Leaving the linear region with respect to lower $|V_{pol}|$ values will result in providing not enough I_{ds} current to drive both devices along with RF couplers (not shown in Fig.6.). This will result in increased settling time for Power out (P_{out}) affecting the 1st stage gain for respective (PA). Fig.7. shows the P_{out} dependency to $|V_{pol}|$.

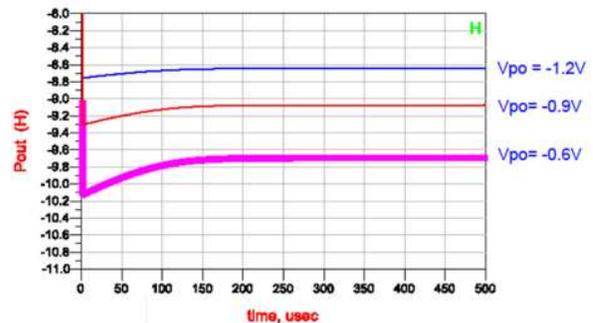


Fig.7. P_{out} response to $|V_{pol}|$

CONCLUSION

In a production environment, regardless of process or design marginalities, Yield for current products

running in-line becomes pivotal to the bottom line of a business. To improve yield based on these variances, we need to control our process to the optimal level. That is, all critical device parameters with respect to Epi and inline process should run on target with Six-Sigma implementation philosophy. Thus, based on the response of P_{out} among different switching mode using BiFET2 technology, FET parameters such as V_{po} , G_m and I_{ds} becomes critical to this application. As the above data shows, (PvT) Power vs Time failure in which P_{out} levels shows longer settling time, Circuit Design improvements along with critical FET parameter improvements with respect to Epi can rectify this problem. The idea is to design Epi for manufacturing (EFM) to produce highest quality products utilizing Qorvo's BiFET2 (GaAs) Technology.

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ACRONYMS

FET: Field Effect Transistor
D-Mode FET: Depletion Mode FET
HBT: Heterojunction Bipolar Transistor
PHEMT: pseudomorphic High Electron Mobility Transistor
 V_{po} : Pinch-off Voltage
GaAs: Gallium Arsenide
PA: Power Amplifier
PvT: Power vs Time Failure
ILPC: Inner loop Power Control
HPM: High Power Mode
MPM: Medium Power Model
LPM: Low Power Mode
 P_{out} : Power-Out
 R_{on} : Open Channel Resistance
EFM: Epi for Manufacturing