A Terahertz Capable 25 nm InP HEMT MMIC Process

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Abstract

A 25nm InP high electron mobility transistor (HEMT) transistor with excellent yield and uniformity was developed for use with the first ever Terahertz Monolithic Integrated Circuit (TMIC) amplifier. The transistor exhibited 3.5 dB maximum available gain at 1Thz and projected f_{MAX} of 1.5THz. Amplifiers designed using this transistor were able to reach 9dB of measured gain at 1.0 THz (1000 GHz) with positive gain extending well above 1.05THz.

INTRODUCTION

The last decade has been characterized by marked improvement in transistor speed capabilities. A variety of MMIC compatible processes, including HEMT and HBT, with a cut off frequency f_T in excess of 600 GHz and a maximum frequency of oscillation f_{MAX} approaching or exceeding 1.0 THz have been reported [1-5]. This improvement in transistor capabilities has enabled a rapid increase in the upper limit of demonstrated integrated circuit amplifier frequencies, with significant milestones at 480GHz[6], 670GHz[7], 850GHz[8], and recently, a demonstration of amplification at 1.0THz [9].

This last milestone was enabled by a newly developed 25 nm InP HEMT and TMIC process. The device is the result of a series of process improvements including gate scaling and epi material enhancement, resulting in a transistor with measured peak transconductance (g_{mp}) > 3.0 S/mm, cutoff frequency f_T of 610 GHz, and a projected f_{MAX} of 1.5 THz.

The next-generation circuits created using this technology will be used in variety of emerging applications at THz frequencies, including high data rate communication systems, atmospheric sensing, planetary exploration, and new classes of imagers.

25NM INP HEMT DEVICE AND TMIC PROCESS

Our main approaches in developing high speed InP HEMTs include transistor gate and layout scaling for parasitic reduction, epi material enhancement for improved electron transport properties, and process improvement associated with the aggressive scaling. The roadmap of this development is summarized in Table I. One can see the transistor performance improvement as a result of each of these advancements.

Table I
Summary of InP HEMT processes developed at Northrop Grumman (NGAS)

Gate length	100nm	70 nm	35 nm	30 nm	25 nm (this work)
Year Introduced	1998	2003	2007	2010	2013
In(x)Ga(1-x)As channel indium composition	60%	75%	100%	100%	100%
Source-Drain Spacing (µm)	2	2	1.5	1.0	0.5
Rc (mΩ.mm)	0.12	0.1	0.04	0.04	0.04
Gmp @ 1V (mS/mm)	1000	1400	2000	2500	3000
f_{MAX} (THz)	0.4	0.6	1.1	1.3	1.5
Associated f_T (THz)	0.2	0.25	0.4	0.5	0.61
Highest frequency amplifier demonstrated (THz)	0.19	0.24	0.48	0.85	1.0
Associated amplifier device width (µm)	30	30	20	14	8

The wafers were grown using molecular beam epitaxy on 3-inch semi-insulating InP substrates. The 25 nm InP HEMT and TMIC process employs an epitaxial profile with InAs composite channel with a total thickness of 95Å, consisting of an InAs layer cladded between two lattice matched $In_{0.53}Ga_{0.47}As$ layers. Si doping planes are placed above and below the channel to enhance sheet carrier concentration (Ns). The final barrier thickness is 20Å, measured from the gate to the Si doping plane. Room temperature mobility of 13000 cm^2/Vs and an Ns of 4.0e12 cm^{-2} are typically obtained by Hall measurements.

A Ti/Pt/Au-based non-alloyed metal stack forms the ohmic contact. An extremely low source resistance (R_s) of 130 mΩ.mm is achieved by scaling the source drain spacing to 0.5 µm shown in Fig. 1b with a low contact resistance (R_c) of 40 mΩ.mm.

The T-shaped 25 nm gate pattern is defined using 100 kV e-beam lithography. The layout is scaled such that the source-drain spacing (0.5um) and gate top (0.4um) are similar in size, requiring precise alignment of the gate with high yield, as shown in Fig. 1b. After the gate pattern is defined, a gate recess is etched using a citric acid based solution. The metal-semiconductor interface is less than 2 nm above the Si doping plane. Special etching procedures were developed to control the etch depth of the transistor, which is critical for dc and RF performance. After the gate recess, a Ti/Pt/Au-based gate

metal is deposited with e-beam evaporation. The devices are then passivated with chemical vapor deposited silicon nitride for improved reliability and robustness. Fig. 1c shows a STEM image of the cross-section of a completed transistor gate.

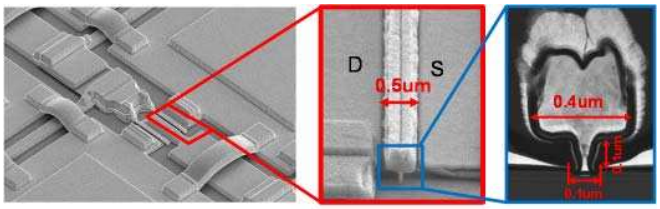

Fig. 1a. SEM image of TMIC; 1b. End view SEM of the transistor with 0.5 µm source-drain distance; 1c. STEM image of the device cross-section.

The TMIC process includes 100 Ω/sq and 20 Ω/sq NiCr thin film resistors, 600 pF/mm^2 metal-insulator-metal capacitors and two levels of metal interconnects. The 2nd metal interconnect can be airbridged. The wafers are thinned to 18µm with fully metalized backside vias. A SEM image of the completed TMIC can be seen in Fig 1a.

Device Characterization and TMIC Amplifier Demonstration

The resulting transistor shows well controlled output conductance to V_{ds}=1.0 V, demonstrating excellent gate control without excessive short channel effect. A peak transconductance (g_{mp}) of 3.1 S/mm is measured at V_{ds}=1 V (Fig. 2). The gate current shows a typical bell shape indicating that it is mainly contributed by impact ionization. The on-state burnout voltage ($BV_{onstate}$) of 2.2 V and off-state burnout voltage ($BV_{offstate}$) of 3.0 V allows for device operation up to V_{ds} of 1.5 V.

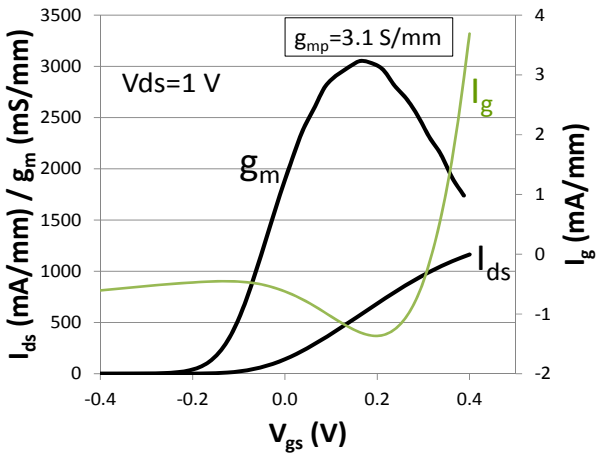

Fig. 2. DC transfer curves of a 2 finger 30 µm device

Fig. 3 shows the MAG/MSG measured on a two finger 10 µm device biased at V_d =1.2 V and I_d=450 mA/mm. The measurement was carried out with the XF system, a WR1.5 and a WR1.0 system for three different frequency bands, i.e. 10 GHz-110 GHz, 500 GHz-700 GHz and 750 GHz-1.0 THz, respectively. ~3.5 dB available gain is measured at 1.0 THz which is sufficient to realize a TMIC amplifier at that frequency. An f_{MAX}=1.5 THz is estimated by extrapolating the 1.0 THz MAG data to unity gain with a slope of -20 dB/decade. The MAG/MSG break frequency is estimated to be between 800 GHz and 1 THz. The corresponding f_T for the transistor is 610 GHz.

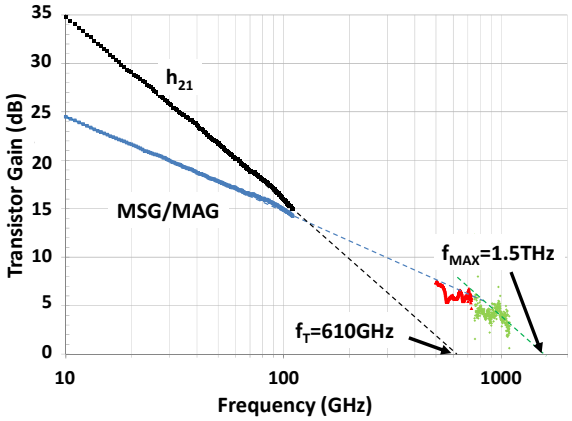

Fig. 3. Measured MAG/MSG and the associated h_{21} of a 2-finger 10 µm device biased at V_d=1.2 V and I_d=450 mA/mm. The dashed lines represent data extrapolations with -20dB/decade and -10dB/decade slopes for the estimation of f_T and f_{MAX}.

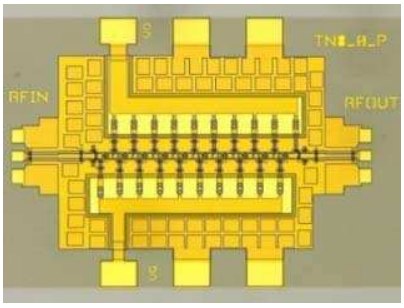

Fig. 4. Microphotograph of 1.0 THz TMIC amplifier.

The transistor technology was further demonstrated by creation of a 10-stage, common source amplifier using 8um transistors consisting of two fingers of 4um each as shown in Figure 4. The TMIC was measured on-wafer using a test set which consists of WR1.0 frequency extenders covering 750-1100 GHz interfaced with a Rohde and Schwarz Vector Network Analyzer. On-wafer probes, similar to the ones used in [8], were developed by the University of Virginia. Calibration is done with on-wafer Thru-Reflect-Line calibration standards fabricated on the wafer.

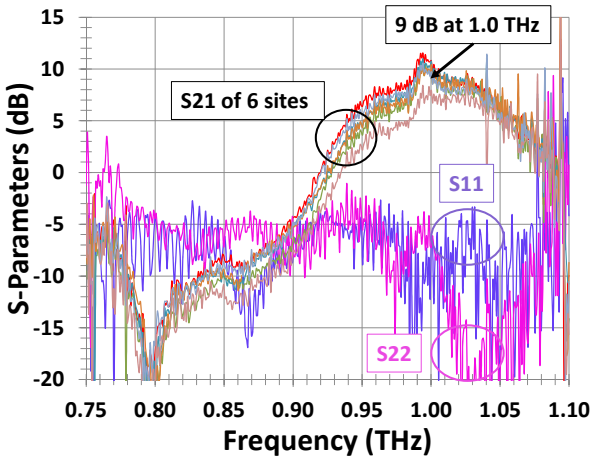

Fig. 5. On wafer measurement results showing 9 dB on-wafer gain at 1.0 THz.

Figure 5 shows the resulting on-wafer measurement, which indicates a gain of 9 dB at 1.0 THz, with positive gain continuing well above 1.05 THz, where 7 dB was measured. This demonstrates the excellent uniformity and yield of the TMIC process.

CONCLUSIONS

A 25nm InP HEMT process with excellent yield and uniformity was developed for use with THz amplifier circuits. The projected >1.0 THz f_{MAX} was demonstrated by performing direct gain measurements at 1.0THz on a 10 stage TMIC amplifier created using the technology. These devices are also expected to operate reliably given the significant commonality in metals, materials and passivation with our space qualified 100 nm InP HEMT technology. This commonality also leads to wafer fabrication cost suitable for a variety of space and airborne applications. This transistor and TMIC technology shows promise in enabling a new suite of components bridging microwave through THz frequencies.

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ACRONYMS

MMIC: Monolithic Microwave Integrated Circuit
TMIC: Terahertz Monolithic Integrated Circuit
HEMT: High Electron Mobility Transistor
HBT: Heterojunction Bipolar Transistor
SEM: Scanning Electron Microscopy
STEM: Scanning Transmission Electron Microscopy
MAG: Maximum Available Gain
MSG: Maximum Stable Gain
NGAS: Northrop Grumman Aerospace Systems