Back Bias Ramping and Photoionization Spectroscopy Analysis of GaN-on-Si HFETs

A. Pooth[1,2*], T. Martin[2], M. J. Uren[1], M. Kuball[1]

[1]Centre for Device Thermography and Reliability, University of Bristol BS8 1TL, UK
[2]IQE (Europe) Ltd., Pascal Close, St. Mellons, Cardiff CF3 0LW, UK
*e-mail: A.Pooth@bristol.ac.uk

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Abstract

In this work, we demonstrate how two methods, namely back bias ramping and photoionization spectroscopy, can be combined to provide important, new information on charge movement in buffer layers of GaN-based Heterostructure-Field-Effect-Transistors. The identification of such effects will help to understand and control the current collapse effect, which is linked to these layers.

INTRODUCTION

GaN-based Heterostructure-Field-Effect-Transistors (HFET) offer significant performance advantages, when compared with silicon devices for next generation power conversion. However, to deliver this performance issues associated with current collapse (CC) and vertical breakdown need to be carefully controlled. Surface related CC can be suppressed by advanced device design [1], leaving the remaining CC related to charge trapping in the buffer layers.

Remaining CC and vertical breakdown are mainly associated with the layers below the 2-dimensional electron gas (2DEG). At present there are some experimental techniques available, in particular back bias ramping [2], to provide details on traps in these layer and to distinguish between good and poor buffer layers. We demonstrate how its combination with spectrally filtered illumination can provide additional critical information on the difference between samples.

EXPERIMENTAL DETAILS

The structures investigated are AlGaN/GaN HFETs with comparable Aluminum concentration and thickness of the AlGaN barrier, resulting in similar carrier concentrations and sheet resistivities. Both samples include a carbon doped buffer. The strain relief layer in sample A consists of a linearly graded AlGaN layer. Sample B contains a multilayer strain relief section with several hetero interfaces and high Al content in some of the layers.

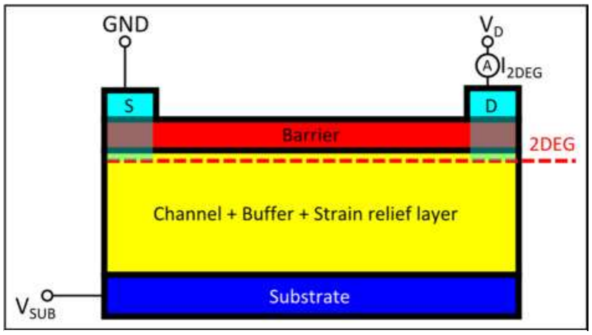

Fig. 1. Experimental setup for back bias ramping.

In the ramped back biasing technique the 2DEG carrier concentration (n_S) of a HFET structure is varied by applying a back-gate voltage (V_{sub}) to a conducting substrate such as p-type silicon. How this voltage is dropped across the layers and the resulting electric field depends on the characteristics of the layers. Monitoring n_S while ramping the substrate bias can therefore be used to gather information about the electrical characteristics of the layers between the 2DEG and the substrate. Fig. 1 describes the setup. The 2DEG current of a structure with no top-gate is measured under a small bias to monitor n_S while V_{sub} is varied. The simple device design with no Schottky type contacts representing low processing requirements enables back bias ramping to be performed early in a manufacturing process.

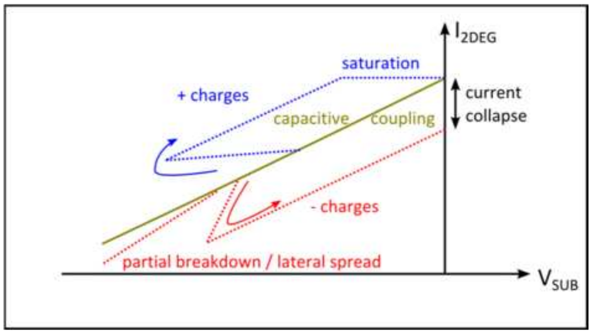

Fig. 2. Schematic 2DEG current vs. substrate voltage plot, illustrating the impact of certain effects on a back bias ramp measurement.

Photoionization is used in this work in combination with the back biasing technique to reveal further information about the buffer layers, which is inaccessible to other techniques or each of the methods on their own. Illumination techniques have succesfully been used to identify and characterize trap levels [3][4] by monitoring the recovery from CC under light, whereas in this work illumination is used during substrate stress conditions that can cause current collapse to gain information about the processes involved. Light source for the experiments was a Xe lamp with a wide spectrum of 250 – 1100 nm spectrally filtered by a prism monochromator.

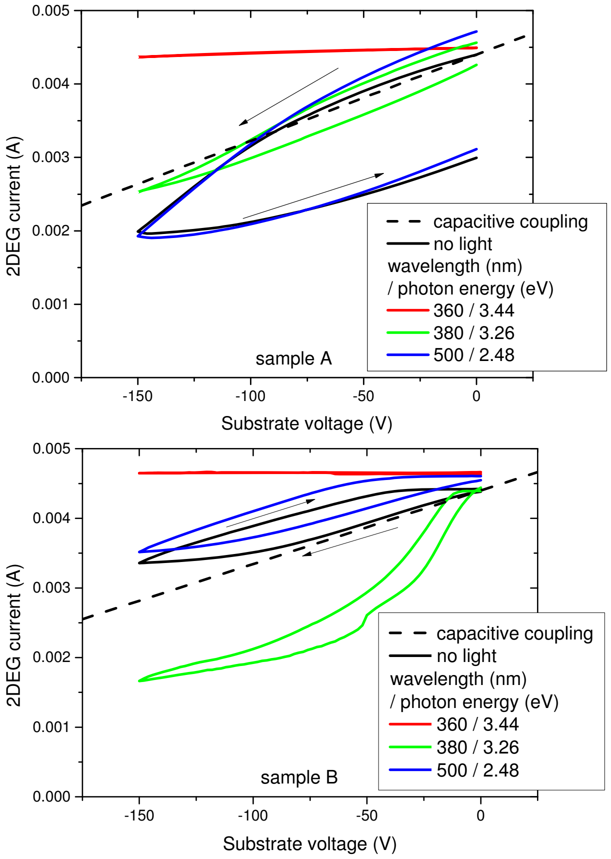

Fig. 3. Back bias ramp curves at different wavelengths. Samples A and B. Ramp rate = 4 V/s, drain voltage = 1 V, measured at room temperature. Arrows indicate the direction for the unlit ramps.

In a back bias ramp measurement an insulating buffer and strain relief layer, with no internal charge redistribution, leads to a linear relation between substrate voltage and n_S, corresponding to capacitive coupling between the conducting substrate and the 2DEG. This behavior is usually observed for small substrate voltages. A redistribution or injection of charges into the buffer layer causes the V_{sub} versus n_S relation to deviate from linear behavior. The range of behavior we have observed is depicted schematically in Fig. 2. Negative charges in the buffer region cause an additional reduction of the 2DEG current, whereas positive charges limit this reduction. Also partial breakdown leading to conductive layers in which charges redistribute [5] or a lateral charge spread along a deep hetero-interface thereby extending the capacitive area in the deeper layers can cause further reductions of the 2DEG current. The effects observed during the application of a substrate bias do not necessarily remain when the back bias is ramped back to 0 V. Positive charges are usually neutralized by electrons injected from the 2DEG in a fast process leaving the 2DEG current at 0 V substrate bias unchanged. Effects that reduce the 2DEG current though can lead to a lasting reduction after the ramp. The latter behavior will also lead to severe current collapse in the real application. Only negative substrate voltages are considered in this paper since these correspond to a power device application with a high positive drain voltage and a grounded substrate.

RESULTS AND DISCUSSION

Back bias measurements for two samples are shown in Fig. 3 both with and without illumination. Clear reduction of current beyond that expected from capacitive coupling is observed for the unlit sample A. This suggests accumulation of negative charges in the vicinity of the 2DEG, which are not neutralized on the return ramp, resulting in a significant current reduction after application of back bias. The curve of unlit sample B shows completely different and much more desirable behavior. The 2DEG current is reduced less than suggested by capacitive coupling, indicating positive charge trapping, resulting in a return at higher current levels, eventually saturating at the initial value due to electron injection from the 2DEG into the buffer. This sample demonstrates the required condition of no net charge trapping following bias stress, in contrast to sample A, which exhibits a current reduction that lasts for 100s of seconds or more and will inevitably result in severe current collapse.

When a back bias ramp is performed under illumination of specific wavelength / photon energy, the resulting current variation can differ substantially. Fig. 3 also shows what happens when samples are illuminated with light of three example wavelengths. Extraction of the current at a specific substrate voltage for all wavelengths tested provides the data for a spectral response curve. -75 V on the return ramp have been chosen for the graphs shown in Fig. 4. Both samples exhibit a high current, well above the unlit level, when illuminated with above GaN bandgap (3.4 eV) photon energy. The large number of generated electron hole pairs is responsible for this effect and effectively screens the 2DEG from the back bias, resulting in the flat ramp curves at 3.44 eV in Fig. 3. At lower photon energies the current level of Sample A drops, saturating close to the value measured without any light. In contrast, sample B shows a significant drop of current at about 3.2 eV to values well below unlit level. This suggests the existence of an ionization process associated with this energy in sample B, potentially the deep donor reported in [6], excitation from a relatively shallow acceptor level to the conduction band as in [3], or from the valence band to a donor level with an ionization energy of 0.2 eV [7]. To cause the drop in current such a process either provides additional negative charges, enables partial breakdown by making a part of the structure conductive, or enhances lateral charge spread at a deep hetero interface.

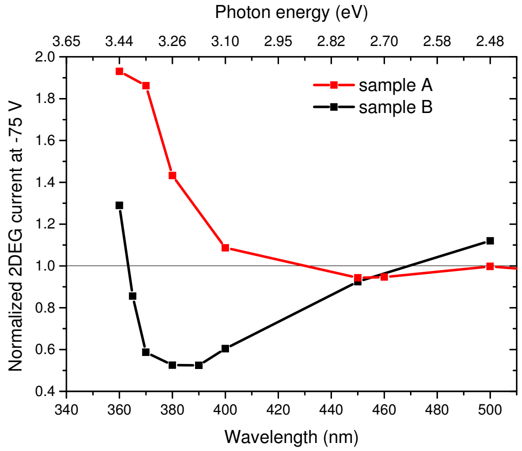

Fig. 4 Photoionization spectral response curves extracted at -75V back bias on the return ramp for the two samples. Normalized to the current measured without light.

A donor level with ionization energy of 0.2 eV has been predicted for carbon doped GaN in [7]. But based on the discussion in [8] it is likely that the donor is overcompensated by an acceptor with ionization energy of 0.9 eV. This donor/acceptor configuration can explain the observed behavior. Fig. 5 describes the charge carrier configurations and movements. Initially all donors are ionized, partially ionizing the acceptor level causing the fermi level to be pinned to the latter. The excitation from valence band to donor leaves a hole in the valence band and a neutralized donor. The donor will immediately ionize again, ionizing an acceptor state. Without any substrate bias applied, the hole will recombine with an acceptor reestablishing the initial state. This explains that no effect of illumination is observed at 0 V back bias. If a substrate bias is present, it will pull the free hole deeper into the structure while the additional negative charge remains on a fixed trap state. This redistribution of charges fed by the 3.2 eV excitation has some analogies with the charge movement observed for sample A in ref. [5]. But the ramp curve for sample B and illumination at 3.26 eV in Fig. 3 shows no lasting reduction. This is due to the barrier at the hetero interface between strain relief section and buffer. The holes stay in the valence band of the buffer, accumulating at the interface and remain available for neutralization of acceptors when the substrate bias is lowered again.

Evidence for the process at 3.2 eV is neither available by photoionization without back bias nor by back bias ramping without illumination for a current collapse free sample. This example shows how the combined methods provide additional information about the structure investigated.

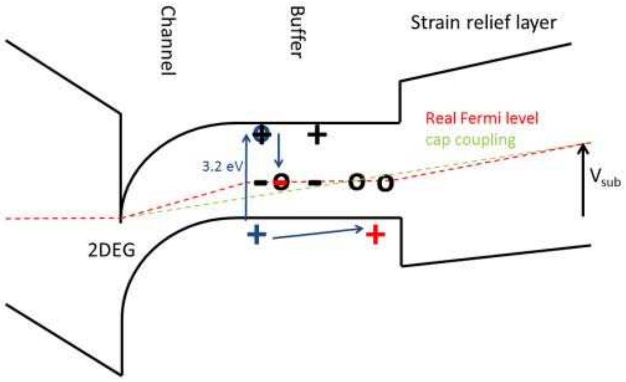

Fig. 5. Schematic band diagram describing the proposed charge movement involving a valence band to donor transition at 3.2eV. Plus signs represent positive charge (holes or ionized donors). Minuses are the equivalent negative charges (electrons or ionized acceptors). Circles are neutral states. Black symbols describe the initial state, red symbols the change in final state. Blue arrows and symbols illustrate excitation, emission processes (vertical arrows), moving charges (horizontal arrow) and intermittent charge states.

CONCLUSION

Back bias ramping has been shown to deliver important information on charging effects in epitaxial layers below the 2DEG and in particular can act as a screening tool to identify epitaxies which demonstrate minimal trapping following bias stress. We also show that photoionization spectroscopy can deliver additional and complementary information to identify charge trapping mechanisms in high performance buffer structures required for GaN power transistors.

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