InP Based Engineered Substrates for CPV Cells Above 46% of Efficiency

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Abstract

By facilitating material recycling, Smart Cut ™ technology enables the cost-effective use of expensive bulk material such as InP. In addition to this cost advantage, different handle substrates such as GaAs, Sapphire or Ge have been evaluated to enable new functions: receiver lift off, lower fragility, better integration. We have demonstrated the recycling of the InP wafer up to 7 times and evaluated up to 10 cycles. Using the InP-on-GaAs engineered substrate combined with direct wafer bonding, Soitec together with Fraunhofer ISE and CEA Leti have demonstrated wafer bonded 4-junction solar cells with highest conversion efficiency of 46.1 %. In parallel, equivalent solar cell performances are demonstrated either on bulk InP substrate or InP engineered substrate.

INTRODUCTION

Indium Phosphide (InP) is a key semiconductor material that enables optical systems to deliver the performance required for data center, metro and long-haul applications. Lasers, photodiodes and waveguides are fabricated on InP. As a semiconductor material, InP can provide all-in-one integrated functionality that includes light generation, detection, amplification, high- speed modulation and switching, as well as passive splitting, combining and routing of light signals [1, 2]. However InP is expensive and fragile which has slowed down further usage for other applications. In the field of CPV cells, advanced triple junction devices reach efficiencies up to 44.4%[3]. Higher efficiencies will require additional junctions. Among the different potential technologies, the combination of junctions lattice matched to InP and GaAs is presented here. This is accomplished by wafer bonding and the use of InP engineered substrates [4].

EXPERIMENTAL

All III-V epitaxial layers were grown in an Aixtron 2800-G4 TM reactor with an 8x4-inch configuration at Fraunhofer ISE. In situ temperature was monitored with a Laytec™ Epi TT system.

At the early steps of the project, GaInAs and GaInAsP junctions were grown on bulk InP substrate. In the targeted product, the InP bulk substrate is replaced by an engineered substrate prepared through the layer transfer of InP on top of a handling substrate. Results presented in this paper are using GaAs as the bottom handling substrate (Fig 1).

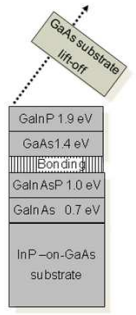

Figure 1. Junctions and substrate for the InP based 4-junction solar cell

The InP substrates used are either n-type or p-type doped (S and Zn) type of (100) orientation and 100mm in diameter. The Smart Cut ™ technology applied to InP layer transfer has been extensively developed by Soitec and CEA –Leti teams. Recently the process window has been explored and a mechanism for the fracture in the InP material following the Smart Cut™ process has been proposed [5]. In parallel a specific implantation tool has been developed for Soitec by Nissin Ion and qualified in the Soitec clean room [6]. H+ implantation was performed with this iG4Hy tool from Nissin ion with an energy of 100 keV and dose varying from $6x10^{16}$ to 10^{17} H^+/cm^2. Implanted InP wafers can be bonded to different sorts of handling substrates like sapphire, Ge or GaAs. Before bonding, the two substrates may be covered with an intermediate additional bonding layer, like PECVD SiO_2 for sapphire. Another option is to bond directly the implanted InP substrate to a conductive substrate such as

GaAs or Ge with a conductive bond. After bonding, a heat treatment in the (200-400°C) range has been applied in order to split the implanted InP wafer, leading to the transfer of a thin InP film (fig.2). Final treatment comprises material removal through CMP to reach the final targeted thickness, final high temperature annealing at 600°C and a final cleaning process that ensures an epi-ready surface. The remainder of the initial InP wafer can be refreshed following a specific wafering process. Wafers are inspected with a Candela CS-20 or with a Tencor 6420. Scanning acoustic microscopy (SAM) was used to check the bonding quality.

All process steps presented below (except solar cell epitaxy and processing performed by Fraunhofer ISE) were performed by Soitec in a dedicated class 100 clean room following proprietary processes. The Soitec clean room is fully equipped for high volume manufacturing of engineered substrates of III-V wafers with diameters of either 100mm or 150mm.

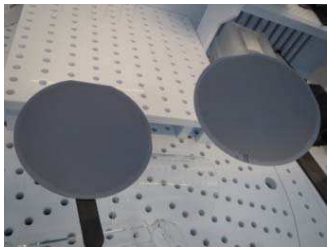

Figure 2. 100mm wafer with thin InP transferred film on a new support substrate (GaAs in this case) following Smart Cut™ technology on the left. Remainig InP wafer is on the right ready for recycling

RESULTS

Characterization of transferred thin InP films by Smart Cut ™ technology before- and after multiple InP wafer re-use

Significant progress has been made on the development of the Smart Cut™ technology with InP bulk wafers. The macroscopic view of the transferred wafer shows a transfer on the full wafer with an edge exclusion of 3mm. The thickness of the transferred InP film is about 300 nm and the root mean square surface roughness is below 0.3 nm as measured by atomic force microscopy.

Crystal quality has been checked through XRD showing similar full-width-half-maximum (FWHM) values to bulk material (Fig.3).

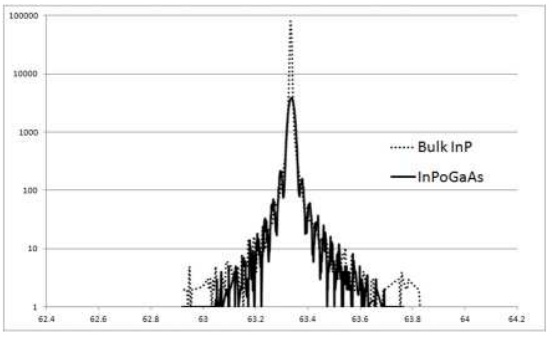

Figure 3. Comparison of XRD rocking curves of InP bulk material and InP-on-GaAs engineered substrate.

InP film thickness uniformity was measured by spectroscopic ellipsometry. With a mean thickness close to 290nm (fig. 4), we can reach a thickness uniformity below 20nm (1sigma).

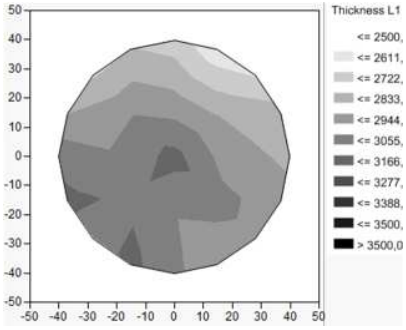

Figure 4. 100mm wafer with thin InP transferred film on GaAs. Thickness is expressed in Angstroms as measured by spectroscopic ellipsometry.

Electrical characterization of the InP-on-GaAs engineered substrate (interface bonding resistivity) is performed following a protocol already presented [6]. For an InP-on-GaAs substrate with a doping level of 4 and 3e18 at/cm^3 for InP and GaAs respectively, an interface resistivity below 10mOhm·cm² is achieved [7]. New results will be presented.

For reaching cost competitiveness, the InP bulk substrate needs to be refreshed after Smart Cut™ and re-used successfully several times. Modeling shows that the contribution of the initial InP wafer cost can be reduced by 80 % after at least 10 cycles. Preliminary tests have shown the potential of InP wafer refreshing up to 10 cycles for the layer transfer of InP on Sapphire [8]. To demonstrate this we have applied a thermal treatment corresponding to 10 cycles of Smart Cut™, and then applied a full Smart Cut™ process. Recently, we have experimentally demonstrated up to 7 full Smart Cut™ cycles and subsequent InP wafer refresh cycles for InP-on-GaAs without any degradation of the starting bulk InP material (see fig.5).

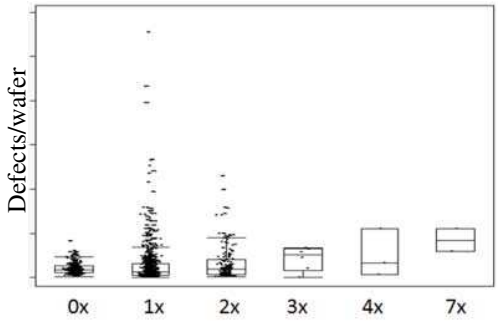

Figure 5. InP bulk defectivity as seen by Candela as a function of refresh cycles. The data at 0x corresponds to fresh InP.

If we check the defectivity of the InP film transferred after 7 cycles of InP donor wafer recycling, we see a quality level in line with the InP film defectivity after layer transfer from a fresh InP bulk material (fig.6).

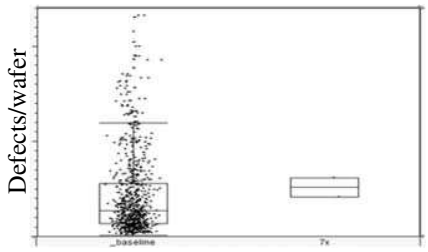

Figure 6. InP layer defectivity of InP-on-GaAs engineered substrate as seen by Candela before epitaxy for a layer transfer from a a fresh bulk InP wafer (baseline) and bulk InP wafer recycled 7 times.

Use of InP-on-GaAs as a template for epitaxy

GaInAs and GaInAsP junctions were grown on a bulk InP substrate for epitaxy development and then tuned for InP-on-GaAs engineered substrate. As shown (fig.7), temperature difference between both substrates processed during the same epitaxy run is below 5K. This shows that epitaxy recipe tuning is easily done when moving from bulk InP substrate to InP-on-GaAs substrate.

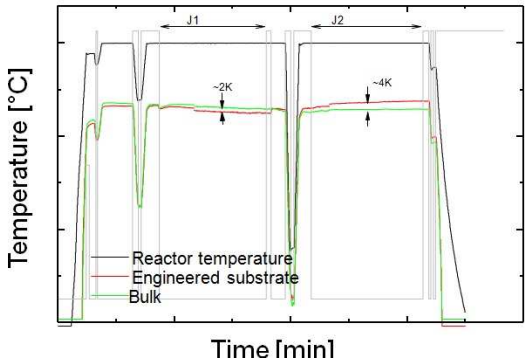

Figure 7. Comparison of in situ temperature monitoring (wafer temperature) during epitaxy growth of GaInAs (J1) and GaInAsP (J2) on bulk InP and InP-on-GaAs (engineered substrate).

Wafer bonded four-junction solar cells.

InP to GaAs wafer bonding technology has been used also for the combination of non lattice matched epitaxial materials (fig.1). Surface cleaning and passivation are key parameters to ensure a clean and efficient bonding interface. Thanks to the use of the Soitec industrial line, the quality of the bonding has been improved and defect free bonding has been obtained. We have demonstrated that the bonding process does not induce any bonding defects as seen by SAM. Remaining defects are linked to epitaxial layer defectivity.

We have reached a low bonding defect density for four junctions cells prepared from both bulk InP wafers and engineered InP substrates (fig.8).

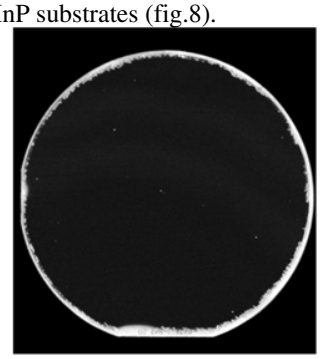

Figure 8. SAM image of a 100 mm diameter sample with four-junctions bonded built on top of an InP-on-GaAs engineered substrate.

The result of this development is the first GaInP/AlGaAs//GaInAsP/GaInAs 4-junction solar cell with a new record efficiency of 46.0% at 508-times concentration of the AM1.5d (ASTM G173-03) spectrum. Details of the cell design and characterization are described in ref [4]. Solar cells from the same epitaxial design have been prepared both on InP bulk and InP-on-GaAs engineered substrates. External quantum efficiencies are similar for both devices and reach values above 90 % (fig.9).

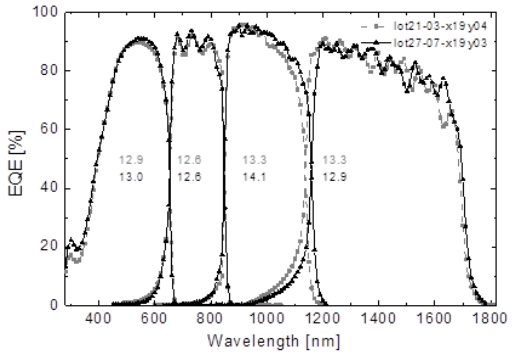

Figure 9. Comparison of external quantum efficiencies for a 4-junction cell grown on a InP bulk substrate (wafer 21-03) or a InP-on-GaAs engineered substrate (wafer 27-07).

In 2015, a higher efficiency has been measured for a 4 junction wafer bonded solar cell grown on InP-on-GaAs. Using the newly developed QuadFlash simulator with an accurate spectrum control to match the photogenerated current densities to AM1.5d conditions, the measurement shows an efficiency of 46.1 % at 312 suns concentration [9].

Growth of epitaxial stack for optoelectronic application

Besides the use of InP-on-GaAs engineered substrate for CPV cells, we have recently explored the fabrication of optoelectronic devices.

Thanks to InPACT and III-V Lab, a multi-quantum well (MQW) structure has been grown by GSMBE on both bulk InP and InP-on-GaAs substrates following the same recipe. Photoluminescence wavelength distributions are presented (fig.10).

(a)

(b)

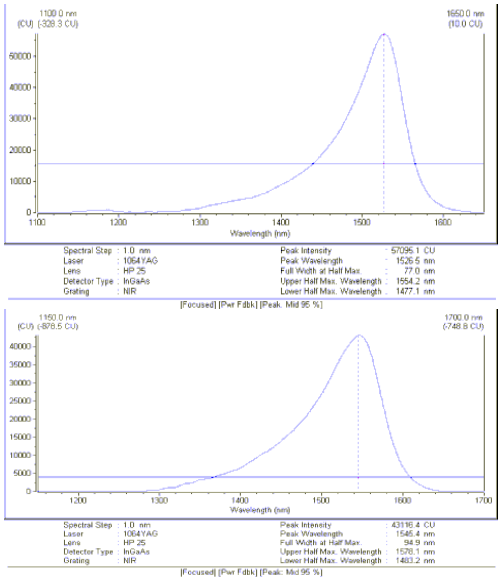

Figure 10. Photoluminescence wavelength distribution of a 1.55µm MQW structure grown by GSMBE epitaxy respectively on bulk InP (a) and InP-on-GaAs (b)

We see that peak PL intensities are close (43 vs 57 au). The slightly higher FWHM for the structure grown on InP-on-GaAs (95 vs 77nm) is linked to edge defects on the InP-on-GaAs since we used a monitor wafer for this first evaluation.

Finally the GaAs substrate can be removed by etching thanks to the etch stop formed by the InP layer. This is of interest for laser structures or photodiodes transfer on SOI, and for reducing the weight of specific devices (e.g.: flexible solar cells).

CONCLUSION

We have developed a Smart Cut ™ technology for InP bulk wafers. Recycling of the bulk InP substrate has been demonstrated up to 7 times. Equivalent efficiencies are measured on both bulk and InP engineered substrates. Finally we have demonstrated external quantum efficiencies above 90 % and efficiencies up to 46.1 % (at 312xAM1.5d) for a wafer bonded GaInP/GaAs//GaInAsP/GaInAs solar cell grown on an InP engineered substrate (InP-on-GaAs). Smart Cut™ technology for InP will also lower the fragility inherent to InP, enable handle substrate removal (GaAs or sapphire lift-off), and enable co-integration with other materials.

ACKNOWLEDGEMENTS

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ACRONYMS

CPV: Concentrated PhotoVoltaic