

# Gallium Nitride P-N Junction Diode Based on Heated Magnesium Implantation and High Temperature Annealing

Sizhen Wang, In Hwan Ji, Alex Huang

FREEDM Systems Center, NC State University, Suite 100, Keystone Science Center, 1791 Varsity Dr. Raleigh, NC 27606  
e-mail: [swang31@ncsu.edu](mailto:swang31@ncsu.edu) Phone: +1(919)995-0818

**Keywords:** GaN-on-Si, Lateral Power Diodes, Magnesium Ion Implantation, High Temperature Annealing

## Abstract

In this paper, we studied p-type GaN materials formed by Mg ion implantation at elevated temperature and thermal annealing. SIMS analysis and electrical test are used to evaluate the p-GaN layer performance. By applying the optimized ion implantation and annealing condition, a lateral P-N junction diode is realized on GaN-on-Si substrate. The device demonstrates breakdown voltage 135V ( $I_{\text{off}}=1\mu\text{A}$ ) and forward current density 191mA/cm<sup>2</sup> at 50V when characterized at 200°C.

## INTRODUCTION

Gallium nitride (GaN), one of the most attractive wide band-gap semiconductor materials, is under intensive investigation for high efficient power switch applications in both industry and academia. Not only lateral GaN HEMT [1], MIS-HEMT [2-3] on hetero-substrate, but also vertical GaN power devices on free-standing GaN substrates are studied worldwide [4-5]. Until now, epitaxy growth with in-situ magnesium doping is the primary approach to form p-type GaN on free-standing GaN or GaN-on-Si substrates. This method can achieve p-type doping concentrations up to  $1\times 10^{18}/\text{cm}^3$  without compromising the surface morphology [10]. But the cost of epitaxy growth is high, and since the p-layer GaN is grown uniformly, it requires additional processing to selectively pattern and remove the p-layer. Therefore it is highly desirable to develop a p-type GaN layer formation technique based on ion implantation and thermal annealing, similar to what is normally used in Si or SiC power devices. So far, limited success has been reported for p-type implantation studies on gallium nitride materials. In 2010, for the first time, G. S. Aluri et al. systematically studied Mg and Be implantation and activation with microwave annealing [6]. In 2014, T. J. Anderson et al. demonstrated a Mg dopant activation rate up to 8.2% using a multiple cycle RTA process [7]. In both cases [6-7], the Mg doped region suffered high resistivity because of a limited activation rate.

This paper reports the development of ion implantation and activation process technology to obtain p-type GaN on Si substrate. Our approach is based on magnesium implantation at elevated temperatures and a high temperature

annealing process. A lateral p-n junction diode is designed as a prototype device to demonstrate the effectiveness of this technology.

## EXPERIMENT DETAILS

The fabrication process started with cost-effective AlGaIn/GaN-on-Si substrates. The GaN epitaxy thickness was  $\sim 3\mu\text{m}$  with unintentional n-type doping  $\sim 1\times 10^{16}/\text{cm}^3$ . After dicing into 16mm $\times$ 16mm square pieces and cleaning with Piranha solution for 15 minutes, the samples were patterned and etched to form mesas for device isolation, and as alignment marks for the following lithography process. Then 50nm LPCVD Si<sub>3</sub>N<sub>4</sub> and 450nm PECVD SiO<sub>2</sub> were deposited on the piece samples, implant areas were opened by photo and wet etching with BoE or DHF solution. The etch process stops at the surface of the Si<sub>3</sub>N<sub>4</sub> because of the high etching selectivity between SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> films. Next, the samples were implanted with magnesium in Nissin's IMPHEAT ion implanter [8], and annealed with EpiQuest's KGX-2000 furnace [9] to activate the dopants. The screening Si<sub>3</sub>N<sub>4</sub> film protects the GaN epitaxial layer from surface degradation during the thermal annealing process. After removing the sacrificial dielectrics and re-depositing silicon nitride as a surface passivation layer, contact windows were defined via a plasma etch process, and 30nm Ni/100nm Au were deposited on samples by lift-off process. Finally, the samples were annealed at 500°C for 10 minutes to form contacts on the implanted region.

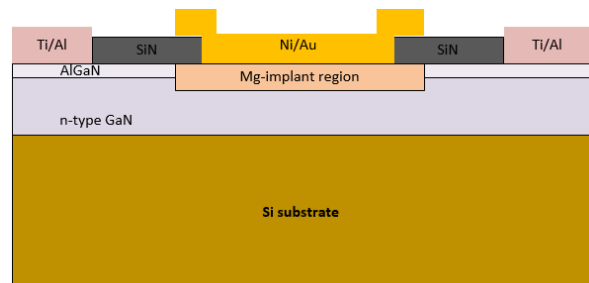


Figure 1. Circular lateral diode structure with anode diameter 236 $\mu\text{m}$

A prototype circular diode structure was designed with a 236 $\mu\text{m}$  diameter anode at the center of Mg implanted region,

5b

and the diode was designed with a field plate to enhance breakdown voltage capability. An outside circular cathode electrode on n-type GaN was formed by depositing Ti/Al/Ni/Au 30/210/30/100nm and alloying at 850C for 30sec in N<sub>2</sub> ambient. Fig. 1 is a side-view schematic of the diode structure. The lateral diodes were characterized with Keithley 4200-SCS up to 200°C.

To optimize the doping process, the samples were processed with splitting Mg implant and anneal conditions as shown in Table 1. Three implantation steps with different ion beam energies and dosages were executed consecutively to form a box profile with 400nm depth. The implant dosage selection is critical to realize p-type GaN with low resistivity. As magnesium is a deep acceptor (~160meV), with an activation rate less than 10% [7], high implant dosage is needed, but the ionization rate is also not high (<10%) and decreases with Mg dopant concentration. Therefore, we tentatively selected a total implanted dosage of  $2.07 \times 10^{15}/\text{cm}^2$ . This high dosage implantation can generate many point defects, dislocations and other cluster defects in the GaN epitaxial layer, but it is still lower than the reported dosage limit of  $3.0 \times 10^{15}/\text{cm}^2$  [10] to fully amorphize the GaN thin film crystal. For compound semiconductors, crystal amorphization during ion implantation posts a big challenge to repair or re-crystallize the lattice during annealing process. To minimize defect generation, in several samples magnesium ions were implanted at an elevated temperature (500°C with a heated chuck), as the dynamic anneal effect during elevated temperature ion implantation can reduce defect density, which was verified in p-type SiC Al implant process [11]. Previous research predicted that the effective activation temperature of Mg implanted ions is higher than 1250°C [12], and the melting point of the silicon substrate is 1410°C. Considering a realistic process margin for the temperature feedback control system of the furnace, a high temperature of 1350°C was selected as one split condition to repair the crystal damage and activate the magnesium dopants.

GaN-on-Si sample annealing at 1350°C is a challenging process since the GaN surface starts to degrade when the temperature is higher than 850°C. MOCVD AlN is usually used as a protection capping layer to prevent nitrogen atom dissociation [7]. In our experiment, a 750°C LPCVD Si<sub>3</sub>N<sub>4</sub> film was used because of its good thermal stability and adhesion with the AlGaN/GaN layer. Both sides of the samples were encapsulated to prevent defect contamination and self-counter-doping from the Si substrate during heating. The thermal expansion coefficient mismatch between silicon and gallium nitride poses another risk when ramping the sealed sample to a temperature higher than the MOCVD epitaxy growth temperature, because the thermal stress can be high enough to generate structural defects.

Table 1. Mg ion implant and anneal split for doping optimization

Split step	Condition	1	2	3
Implant steps (total dose 2.07E15/cm2)	110KeV 8.3E14/cm2(RT, 7 tilt)	•		
	55KeV 8.3E14/cm2(RT, 7 tilt)	•		
	25KeV 4.1E14/cm2(RT, 7 tilt)	•		
	110KeV 8.3E14/cm2(500C, 7 tilt)		•	•
	55KeV 8.3E14/cm2(500C, 7 tilt)		•	•
	25KeV 4.1E14/cm2(500C, 7 tilt)		•	•
Activation Anneal	850C 60sec		•	
	1350C 60sec	•		•

## RESULTS AND DISCUSSION

Electrical performance of the Mg-doped AlGaN/GaN layers is evaluated using a Van der Pauw structure, and the results are shown in Fig. 2. For all three samples, current conduction is non-linear and symmetric under both positive and negative bias. By comparing sample 2 and 3, it can be seen that 850°C annealing is not effective at activating the dopant, while 1350°C annealing for 60sec shows improved current conduction performance. Comparing the sample 1 and 3 shows the sample with elevated implantation temperature at 500°C demonstrates more than three times the current density when biased at 100V. This current conduction enhancement is due to the lower implantation induced lattice damage when doped at 500°C instead of room temperature, showing that dynamic annealing [11] is also effective for the case of Mg implanted into GaN epitaxial layers.

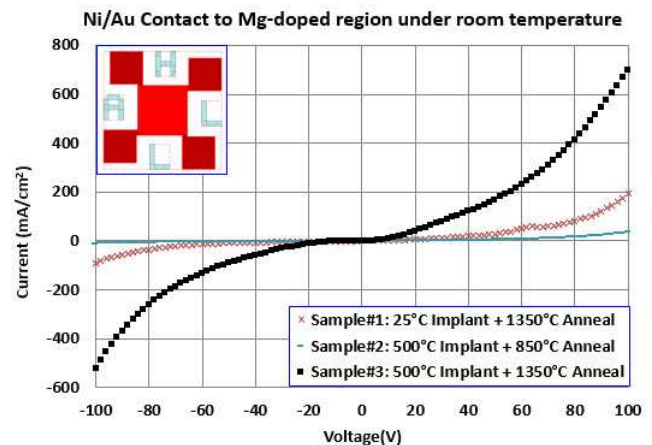


Figure 2. I-V curve test with Van der Pauw structure for different Mg implant and anneal condition samples

After thermal annealing for 60 seconds, samples were sent for ToF-SIMS analysis. The extracted Mg doping profile in three samples are shown in Fig. 3. The peak concentration of Mg  $2 \times 10^{20}/\text{cm}^3$  is located at the interface between Si<sub>3</sub>N<sub>4</sub> and AlGaN layer, which is favorable for p-type ohmic contact formation. Among all three sample, there

is no obvious difference of Mg doping profile after thermal activation with 60sec, so it can be concluded that no Mg diffusion or redistribution occurred with those thermal conditions, which is consistent with results from J.C. Zolper [12].

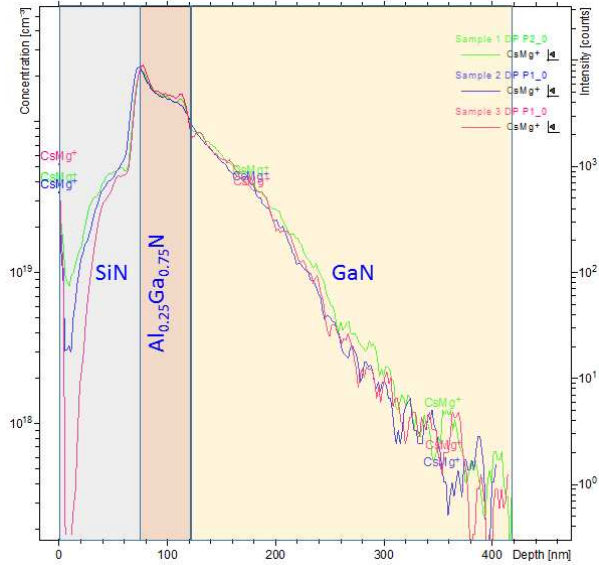


Figure 3. ToF-SIMS analysis showing magnesium dopant profile comparison after annealing.

Optical inspection after the thermal annealing process reveals macro extend defects on the epitaxial surface, as shown in the right bottom alignment mark pattern in Fig. 4. After the annealing process, the sample does not retain its original size, which can be seen from the mismatch of the alignment marks at each corner of the sample (Fig. 4). It is estimated that the annealed GaN-on-Si expands at least 3µm in both horizontal and vertical directions. This deformation made later photo alignment processing quite challenging.

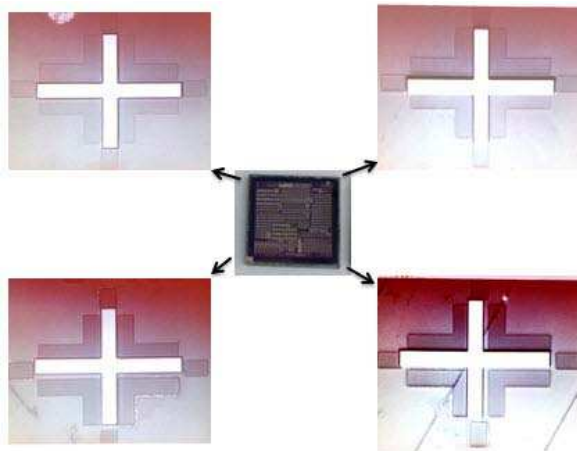


Figure 4. Annealed sample alignment marks show mismatch with target on the mask. The four alignment marks are located at each corner of the sample.

Although samples with 500°C implantation and 1350°C annealing demonstrated the best performance, device grade ohmic contacts have not been realized at room temperature due to limited dopant activation rate. TLM I-V measurements were conducted to check the effect from high temperature (Fig. 5). The current density increased four orders of magnitude when increasing the characterization temperature from 25°C to 200°C. When plotted in linear scale, at 200°C, the TLM structure demonstrate a linear increase of current conduction with differential resistance 11.20MΩ.

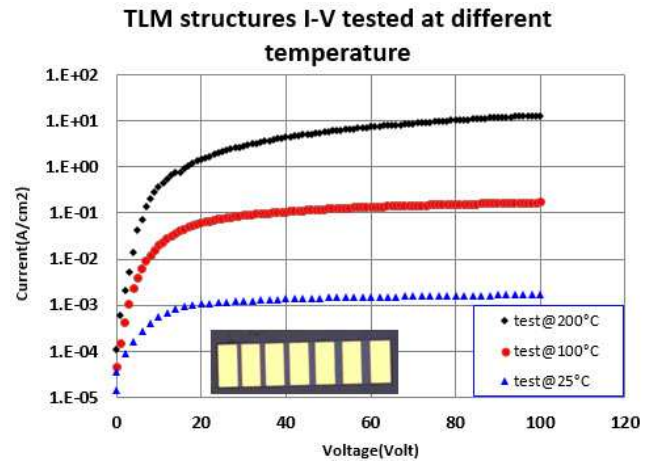


Figure 5. TLM structure I-V measured at different temperature

The circular p-n diode layout is shown in the upper left of Fig. 6. By applying our developed Mg doping technology, P-N lateral diodes on GaN-on-Si were fabricated and characterized at different temperatures (Fig. 6). At room temperature, the diode current is very low which is related to low magnesium dopant activation rate. As test temperature increase, the Mg dopant ionization can increase. Diode behavior was demonstrated with breakdown voltage of 135V ( $I_{off}=1\mu A$ ) when it was tested at 200°C. The conduction current density (normalized to sidewall junction area) increased linearly with forward bias. At 50V, a current density 191mA/cm<sup>2</sup> was achieved.

5b

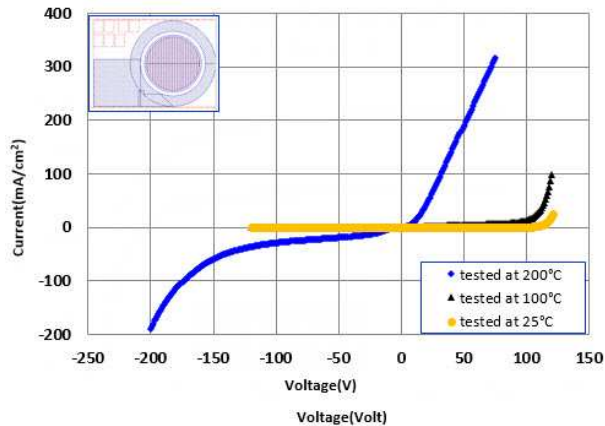


Figure 6. Circular P-N diode static I-V test at different temperatures

## CONCLUSIONS

With magnesium implantation at elevated temperatures and high temperature annealing, we have developed a process technology to realize p-type GaN on cost effective GaN-on-Si substrate. Several critical process steps were discussed and process challenges which deserve further study were pointed out. Finally, by applying the implant and annealing approach, prototype lateral PN diodes with breakdown voltages around 135V (at 200°C) were demonstrated. Although further process tuning is needed, the successful application of implantation formed p-GaN to demonstrate prototype lateral GaN diode paves the way for realizing other types of power devices.

## ACKNOWLEDGEMENTS

The authors would like to thank NISSIN Ion Equipment Co. Ltd., EpiQuest Inc., and Toyo Tanso Co. Ltd. for providing assistance with heated Mg ion implantation, and Mg doped sample annealing.

## REFERENCES

- [1] Mishra, Umesh K.; et al. "AlGaIn/GaN HEMTs-an overview of device operation and applications," in *Proc. of the IEEE*, vol.90, no.6, pp.1022-1031, Jun 2002.
- [2] Ye, P. D., et al. "GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al<sub>2</sub>O<sub>3</sub> as gate dielectric." *Applied Physics Letters* 86.6 (2005): 63501-63501.
- [3] Yue, Yuanzheng, et al. "AlGaIn/GaN MOS-HEMT With Dielectric and Interfacial Passivation Layer Grown by Atomic Layer Deposition." *Electron Device Letters, IEEE* 29.8 (2008): 838-840.
- [4] D. Disney, et al. "Vertical Power Diodes in Bulk GaN", *ISPSD*, pp. 59-62, 2013,
- [5] H. Ohta, et al. "Vertical GaN p-n Junction Diodes with High Breakdown Voltage Over 4kV", *Electron Device Letter, IEEE* 36, 11(2015), pp. 1180-1182.
- [6] Geetha S. Aluri, et al., "Microwave annealing of Mg-implanted and in situ Be-doped GaN", *Journal of Applied Physics* 108, 083103 (2010).
- [7] T. J. Anderson, et al., "Activation of Mg implanted in GaN by multicycle rapid thermal annealing" *Electronics Letters*, Vol. 50, no. 3, p. 197 – 198. 2014.

- [8] T. Igo, et al, "Development of Medium Current Ion Implanter "IMPHEAT" for SiC", *AIP Conf. Proc.* 1321, 388 (2011)
- [9] <http://www.epiquest.co.jp/pdf/kgx-2000.pdf>
- [10] Omar Manasreh, ed. "III-Nitride Semiconductor: Electrical, Structural, and Defects Properties", Elsevier 2000,
- [11] Carl J. MeHargue, et al., "Ion implantation effects in Silicon Carbide", *Nuclear Instrument and Methods in Physics Research B*, 80/81, pp. 889-894 (1993).
- [12] J. Edgar, ed. "Properties, Processing and Applications of Gallium Nitride and Related Semiconductor", IET, 1999,

## ACRONYMS

GaN: Gallium Nitride  
 SiC: Silicon Carbide  
 AlN: Aluminum Nitride  
 HEMT: High Electron Mobility Transistor  
 MIS-HEMT: Metal-Insulator-Semiconductor HEMT  
 PECVD: Plasma Enhanced Chemical Vapor Deposition  
 MOCVD: Metal Organic Chemical Vapor Deposition  
 LPCVD: Low Pressure Chemical Vapor Deposition  
 TLM: Transmission Line Measurement  
 ToF-SIMS: Time of Flight Secondary Ion Mass Spectrometer