

# Plasma-Enhanced ALD for Improved MOS Interfaces in III-V Semiconductors

V. G. Rezazadeh<sup>1</sup>, K. M. Bothe<sup>1</sup>, A. Afshar<sup>2</sup>, K. C. Cadien<sup>2</sup>, D. W. Barlage<sup>1</sup>

<sup>1</sup>Dept. of Electrical and Computer Engineering, University of Alberta

<sup>2</sup>Dept. of Chemical and Materials Engineering, University of Alberta  
9211 116 Street NW, Edmonton, AB, Canada, T6G 1H9

e-mail: vrezazad@ualberta.ca, barlage@ualberta.ca Phone: +1 (780) 492 4081

**Keywords:** Gate oxides, InP, GaN, MOSFET, PEALD, ZrO<sub>2</sub>

## Abstract

To enable scalable MOSFET technology in III-V semiconductor platforms, high quality semiconductor-oxide interfaces are essential. In this work, a novel low-temperature plasma-enhanced atomic layer deposition (PEALD) technique was applied to deposit nanoscale high-k dielectrics on several III-V substrates, including InP, GaAs, InAs, and GaN. Approximately 7 nm of ZrO<sub>2</sub> was grown and patterned to form MOSCAP structures, which were subsequently analyzed through electrical characterization to evaluate dielectric and interface quality. The oxide films fabricated were found to have interface trap densities ranging from 10<sup>10</sup>-10<sup>13</sup> eV<sup>-1</sup>cm<sup>-2</sup>, and showed high capacitance density (~2.5 μF/cm<sup>2</sup>). Simulated InP MOSFET devices using these experimental values demonstrated high ON current and cutoff frequencies.

## INTRODUCTION

With the rapid introduction of efficient atomic-layer deposition (ALD) techniques for high-k oxides over the past decade, III-V semiconductors have become serious potential candidates for future generations of high-performance MOSFETs, in particular with respect to large-scale integration. While the commercial development of MOSFETs in non-silicon platforms has been lacking, III-V semiconductors are attractive for a multitude of applications, owing to their higher carrier mobility and higher breakdown voltage compared to silicon [1]. In addition to improved material properties, semi-insulating InP, GaAs and InAs substrates can be used in IC manufacturing, reducing device parasitics dramatically and enabling high-quality microwave devices [2]. In this work, we aim to implement a suitable high-k gate dielectric, ZrO<sub>2</sub>, and subsequently analyze its chemical compatibility with the most prominent III-V semiconductors.

While the prospect of functional oxide-semiconductor interfaces in the III-V platform is enticing, the undesirable chemical nature of many of these semiconductors presents significant challenges in oxide deposition [3]. To date, efforts

in ALD high-k oxides on III-V have produced mainly poor quality interfaces with a large density of oxide interface traps (D<sub>it</sub>), responsible for deleterious effects on MOS devices such as Fermi-level pinning [4]. A significant component in the formation of these traps is the chemical nature of the native oxide layer formed on the surface of the semiconductor in equilibrium conditions (see Figure 1).

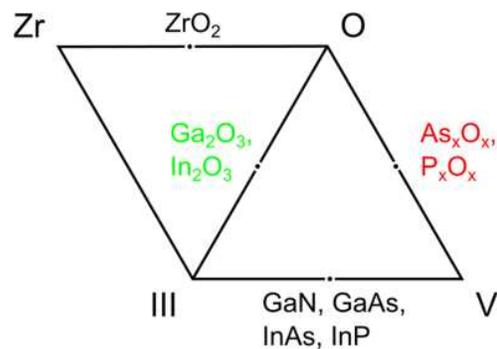


Figure 1: The chemical phase diagram between group III elements, group V elements, elemental zirconium, and elemental oxygen. Formed compounds are shown along the sides of the triangles [3].

This presents serious issues in semiconductors such as GaAs and InAs, where unstable As oxide compounds can form and additionally cause parasitic gate conduction [5]. In order to mitigate the effects of these compounds and deposit high-quality high-k oxides on III-V materials, it is necessary to examine the dynamics of ALD deposition and substrate surface chemistry. By applying conditions favorable to the growth of high-k compounds and suppressing the growth of native oxides on III-V compounds using a mixture of low temperature and surface treatments, this work aims to demonstrate a suitable III-V oxide interface and enable the construction of MOSFETs in these material systems.

## FABRICATION AND PROCESSING

Recent work by several groups has shown that surface plasma treatment in combination with the ALD process can produce higher-quality semiconductor-oxide interfaces with

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reduced  $D_{it}$  in III-V materials, owing to the passivation of native metallic and oxide compounds [6][7]. One such example is an oxygen plasma-enhanced ALD process, which combines short pulses of oxygen with high-k ALD organometallic precursors. This technique has been shown to generate high-quality MOS interfaces on GaN previously [7]. In this work, we applied the fabrication process described in [7] but using a series of different III-V materials including GaAs, InAs, and InP.

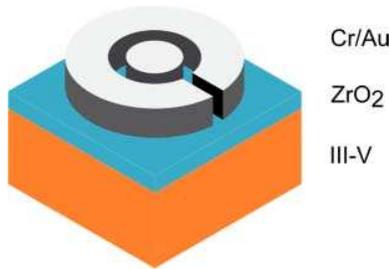


Figure 2: Physical layout of planar MOSCAP structures fabricated on III-V substrates, showing the layer stack of each device.

Using n-type substrates including silicon-doped (100) GaAs ( $N_D = 1 \times 10^{18} \text{ cm}^{-3}$ ), silicon-doped (100) InAs ( $N_D = 1 \times 10^{18} \text{ cm}^{-3}$ ), and sulfur-doped (100) InP ( $N_D = 1 \times 10^{18} \text{ cm}^{-3}$ ), planar MOSCAP devices were fabricated, shown in Figure 2. Before processing, wafers were individually cleaned using a two-step acetone and IPA rinse.  $\text{ZrO}_2$  was then deposited on the aforementioned substrates using an oxygen plasma-enhanced process at a temperature of 100 °C in a Kurt J. Lesker ALD reactor, with a chamber pressure of 1 Torr. A film consisting of 40 cycles of oxide was deposited, alternating between tetrakis(dimethylamido)-zirconium and oxygen pulses. Using in-situ ellipsometry data, the thickness of the  $\text{ZrO}_2$  as-deposited was found to be 6.87 nm. After oxide deposition, annular metal contacts were formed by ultrasonic acetone lift-off of RF sputtered chrome and gold films defined through contact lithography.

#### ELECTRICAL DATA AND CHARACTERIZATION

After MOSCAPs were successfully fabricated, a series of electrical measurements were conducted using a Keithley 4200-SCS analyzer unit to extract information about the quality of the  $\text{ZrO}_2$  films deposited. In order to obtain  $D_{it}$  values from the interfaces of MOSCAP devices, two methods were used, namely the low-frequency capacitance-voltage hysteresis and capacitance-frequency conductivity extraction methods [8]. Applying these methods to the series of substrates processed,  $D_{it}$  values were obtained for GaAs, InAs, and InP, with previous results on GaN included for comparison. Of these materials, GaN showed the lowest overall  $D_{it}$  through both methods applied (on the order of  $10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ ), while GaAs showed the highest overall  $D_{it}$  (on the order of  $10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ ). By this measure, films on GaN and

InP compare favorably to high-k dielectrics currently used in production Si devices, which have  $D_{it}$  figures on the order of  $10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$  [9]. Both GaN and InP demonstrated efficient gate control using the  $\text{ZrO}_2$  dielectric, with clear modulation of the capacitance with respect to voltage. Furthermore, the InP MOSCAPs examined demonstrated charge-carrier inversion in the reverse bias region of the capacitance-voltage plot. All of the semiconductors with the exception of InAs showed a fairly high peak capacitance density ( $\sim 2.5 \mu\text{F}/\text{cm}^2$ ). With the combination of  $D_{it}$  and peak  $C_{ox}$ , these results exceed the benchmark of previous records for high-k films on InP ( $\sim 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ ) [10].

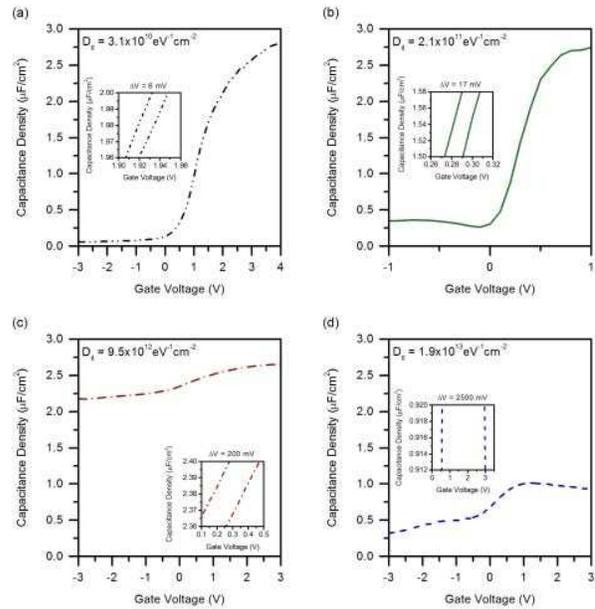


Figure 3: The low frequency (10 kHz) CV characteristics for  $\text{ZrO}_2$  MOSCAPs on different compound semiconductors; (a) GaN, (b) InP, (c) InAs, and (d) GaAs. The corresponding density of interface traps were extracted from the forward/reverse biased C-V hysteresis.

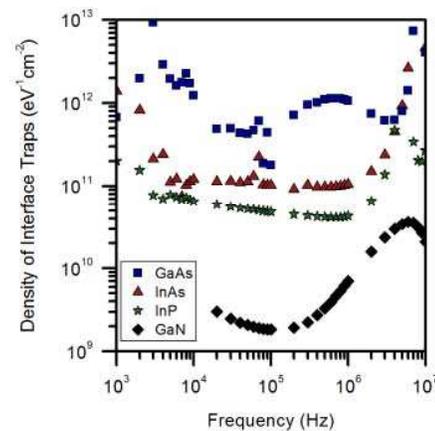


Figure 4: The interface trap density for the  $\text{ZrO}_2$  MOSCAPs obtained from the conductance-frequency spectrum.

TABLE I  
D<sub>IT</sub> VALUES OF ZrO<sub>2</sub> ON VARIOUS III-V MATERIALS

Material	Conductance Method (eV <sup>-1</sup> cm <sup>-2</sup> )	Hysteresis Method (eV <sup>-1</sup> cm <sup>-2</sup> )
GaAs	1.9x10 <sup>13</sup>	1.9x10 <sup>13</sup>
InAs	4.6x10 <sup>12</sup>	9.5x10 <sup>12</sup>
InP	4.5x10 <sup>11</sup>	2.1x10 <sup>11</sup>
GaN	3.6x10 <sup>10</sup>	3.1x10 <sup>10</sup>

In addition to capacitance-voltage measurements, the oxide leakage current was measured for each MOSCAP, with the results shown in Figure 5. While GaN/ZrO<sub>2</sub> offers an excellent D<sub>it</sub> figure, it does not show as low of leakage current due to a smaller band offset and favorable effective mass ratios. In contrast, InP shows similarly low D<sub>it</sub> but a lower leakage current because of a higher potential barrier formed by band offsets (lower electron affinity). Despite this, both of these material systems show lower leakage current than InAs, which showed significantly higher D<sub>it</sub> and is thus most likely suffering from a trap-assisted tunneling condition.

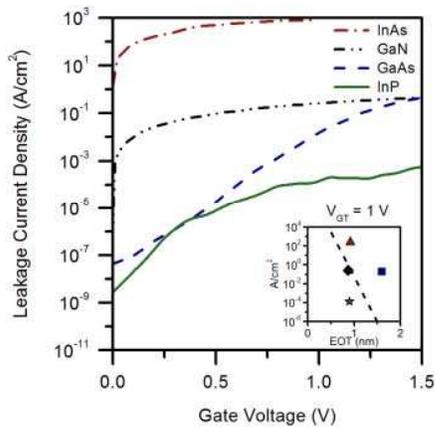


Figure 5: The forward bias leakage current and sub-threshold slope of the ZrO<sub>2</sub> MOSCAPs on InAs (red), GaN (black), GaAs (blue) and InP (green). The inset compared the MOSCAPs equivalent oxide thickness with respect to tunneling current at V<sub>GT</sub> = 1 V. The dashed line represents the accepted HfO<sub>2</sub> EOT tunneling current.

Finally, field-effect mobility extraction was also performed using the capacitance-voltage results for each material system in a transmission-line model, used previously for GaN devices [11]. However, accurate measures for charge density and thus mobility could not be obtained for GaAs and InAs devices due to the lack of charge modulation. For InP/ZrO<sub>2</sub>, parameters were properly extracted and the low field mobility was measured via the frequency sweep technique to be 1060 cm<sup>2</sup>/Vs. We used this value to calibrate simulations and evaluate device suitability for RF applications.

## MOSFET SIMULATION

Following the extraction of electrical characteristics, a sample InP MOSFET was constructed in Crosslight TCAD software using the experimental dielectric characteristics obtained. This simulation was designed to analyze the performance of an entire high-mobility III-V MOSFET device using real oxide parameters, as opposed to analyzing the semiconductor-oxide interface in isolation. Of the materials tested, InP was chosen for the simulation on the basis of its low trap density interface (compared to InAs and GaAs), as well as its beneficial properties at microwave frequencies. The device simulated incorporated a 50 nm thick regrown n-type In<sub>0.53</sub>Ga<sub>0.47</sub>As source/drain (N<sub>D</sub> = 1x10<sup>20</sup> cm<sup>-3</sup>) in a 90 nm gate length structure, using an EOT corresponding to the thickness specified in the ITRS Roadmap for high-performance processes (1.2 nm) [12]. In order to examine the effects of varying source-drain regrowth geometries on device performance, several structures were defined. Between each structure, a source-drain recess etch of different depth was applied, aiming to show the effects of increased gate planarization.

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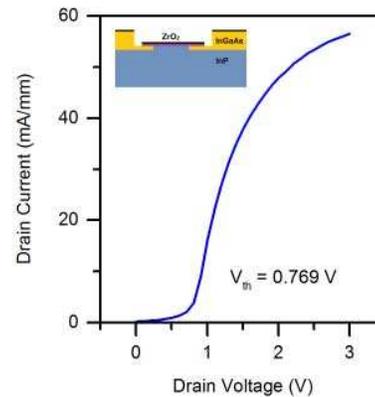
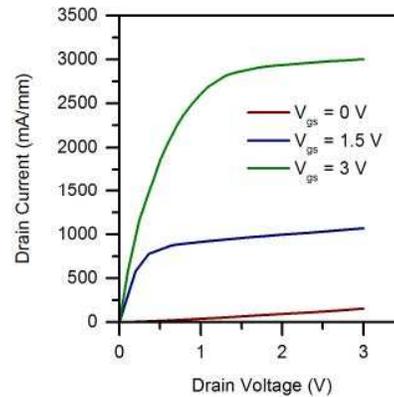


Figure 6: I<sub>ds</sub>-V<sub>ds</sub> and I<sub>ds</sub>-V<sub>gs</sub> curves of a 90 nm simulated InP MOSFET using extracted values of the experimental ZrO<sub>2</sub> high-k dielectric. The I<sub>ds</sub>-V<sub>gs</sub> curve is measured at V<sub>ds</sub> = 0.05 V. The optimized device structure is shown in the inset.

After simulation, a combination of electrostatic, DC, and AC device parameters were obtained through the TCAD software solver and analyzed. As the gate and source-drain regions became more planar with increasing etch depth, there was a noticeable increase in both cutoff frequency and drain current. This effect is likely due to an increase in channel control and inversion charge transport efficiency between the channel and source-drain. A fully-recessed source-drain was found to produce the most optimal results, with an on current of  $3.00 \times 10^3 \text{ mAmm}^{-1}$  at  $V_{ds} = 3 \text{ V}$  and a cut-off frequency of 117 GHz. On the other hand, the non-planarized approach utilized often with regrown InGaAs source-drains [13] showed decreased performance, with an on current of  $2.08 \times 10^3 \text{ mAmm}^{-1}$  at  $V_{ds} = 3 \text{ V}$  and a cut-off frequency of 55.7 GHz.

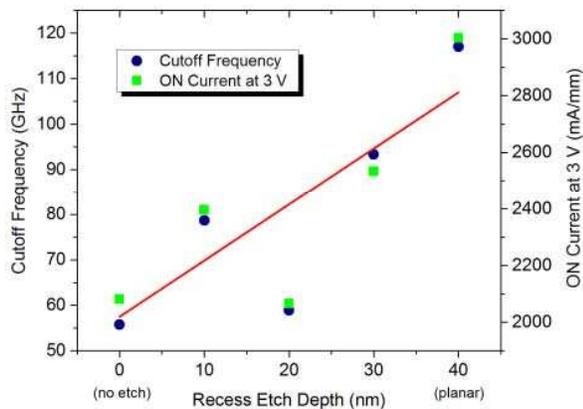


Figure 7: Cutoff frequency and peak ON currents of simulated InP MOSFETs with varying gate overlap recess etch depths in the source-drain regions.

## CONCLUSION

Using a low-temperature, plasma-enhanced atomic layer deposition technique,  $\text{ZrO}_2$  MOSCAP devices were fabricated on selected III-V substrates, including GaAs, InAs, and InP. With this process, oxide-semiconductor interfaces fabricated were found to have improved capacitance density and reduced oxide interface trap density, opening potential applications in III-V MOSFET technology. In order to examine the performance of future devices, various InP MOSFETs were simulated in TCAD software, incorporating real material and interfacial parameters extracted from the experiments conducted. The MOSFETs shown demonstrated high drive current and cut-off frequencies, with a fully planarized source-drain and gate producing the best results. These results demonstrate the significant potential for InP MOSFETs in microwave and millimeter-wave applications.

## ACKNOWLEDGEMENTS

The authors are thankful to the University of Alberta Nanofab for their assistance in processing and fabrication.

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## ACRONYMS

EOT: Equivalent oxide thickness  
MOSCAP: Metal oxide semiconductor capacitor  
MOSFET: Metal oxide semiconductor field-effect transistor  
TCAD: Technology aided computer design  
 $\text{ZrO}_2$ : Zirconium oxide