Inductively Coupled Plasma Dry Etching Process Development for > 50 Gb/s 850 nm Oxide-Confined VCSELs

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Abstract

We develop the ICP dry etching process for our high speed 850 nm oxide-confined VCSELs. The ICP etching provides the capability of low pressure etching for high etching rate and better etching profile. There are 3 pairs of $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$ below the active region, and the rest of the n-type bottom DBR is made of $AlAs/Al_{0.12}Ga_{0.88}As$. Because of the fast oxidation of the AlAs layers, the ICP etching needs to ensure those layers are not exposed. However, the $Al_{0.98}Ga_{0.02}As$ layers on the DBR mesa need to be exposed properly for a uniform oxidation. The fabricated VCSEL shows a high modulation bandwidth of 29.15 GHz and demonstrates error-free (BER < 10^{-12}) transmission at 57 Gb/s data rate.

Introduction

Oxide-confined 850 nm vertical cavity surface-emitting lasers (VCSELs) are the most cost effective solution for short-haul optical interconnects because of their low threshold and high direct modulation bandwidth capability. The native oxide was first used in edge-emitting diode lasers [1] and then VCSELs [2] for electrical and optical confinement. Besides electrical carrier and optical modal confinement, the oxide apertures formed by lateral oxidation also provide scaling capability for VCSELs. Directly modulated 850 nm oxide-confined VCSELs with error-free data transmissions from 40 to 57 Gb/s have been demonstrated [3-7]. The 850 nm oxide-confined VCSELs are the current standard devices for the high speed optical transceivers for the short-haul data links in the data centers. The current transceiver products require each VCSEL channel to operate 25-28 Gb/s, and VCSELs are put into arrays for 100 Gb/s transmission. Following the trend of doubling the transmission data rate every generation, the 850 nm VCSELs are expected to operate above 50 Gb/s in the near future.

In this work, we report the inductively coupled plasma (ICP) dry etching process development for InGaAs quantum-well VCSELs showing a record performance of 57 Gb/s error-free data transmission and a high modulation bandwidth of 29.15 GHz.

Device Fabrication and Process Development

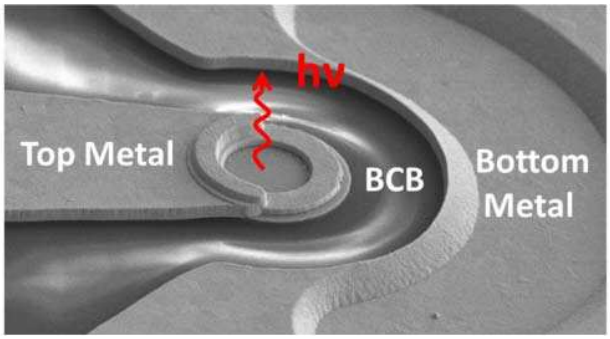

Figure 1. A SEM image of the top view of a fabricated 850 nm oxide-confined VCSEL.

The VCSEL material is grown by metalorganic chemical vapor deposition (MOCVD), and the layer structure of the VCSEL (from bottom to top) consists of 26 pairs of n-type $AlAs/Al_{0.12}Ga_{0.88}As$ then 3 pairs of $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$ as the bottom distributed Bragg reflector (DBR) layers; above the bottom DBR stack is the multiple quantum well (MQW) active region with 5 $In_{0.072}Ga_{0.928}As/Al_{0.37}Ga_{0.63}As$ QWs and the top p-type DBR which includes 2 pairs of $Al_{0.98}Ga_{0.02}As/Al_{0.12}Ga_{0.88}As$, 4 pairs of $Al_{0.96}Ga_{0.04}As/Al_{0.12}Ga_{0.88}As$, and 14 pairs of $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$, and finally a p-type GaAs contact layer. The fabrication starts with top p-type Ti/Pt/Au contact metal evaporation. Then, SiN_x is deposited and patterned with photolithography and CF_4 reactive ion etching (RIE). The patterned SiN_x serves as a hard mask for the following inductively coupled plasma (ICP) dry etching to create the top DBR mesa. After the ICP etching, the sample is sent into a wet furnace filled with water vapor and N_2 carrier gas for lateral oxidation. The exposed high Al-content ($x > 0.9$) $Al_xGa_{1-x}As$ layers on the DBR mesa will be oxidized. The oxidation rate is calibrated beforehand, and the oxidation time is calculated according to the targeted oxide aperture diameters. The bottom n-type AuGe/Ni/Au contact metal is evaporated and then alloyed. The benzocyclobutene (BCB) is spun onto the sample for planarization and passivation. A BCB etchback is done by RIE with CF_4/O_2, and later the BCB via hole etching is also performed with CF_4/O_2 in RIE. Finally, Ti/Au M1 metal

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interconnects and probe pads are evaporated. A scanning electron microscope (SEM) top view of a fabricated device is shown in Figure 1.

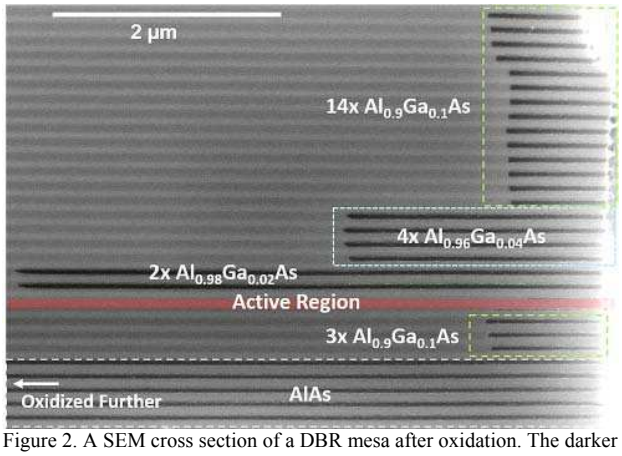

Figure 2. A SEM cross section of a DBR mesa after oxidation. The darker lines are the oxidized region.

ICP (or ICP RIE) dry etching is used in the fabrication process because it can etch the semiconductor under lower pressure as compared to a RIE system. Different from a RIE system with 2 parallel electrodes on the showerhead and the platen, the ICP RIE system includes a second RF source, i.e. the ICP, to increase the ion density in the chamber, so the etching can be performed at low chamber pressure for faster etching and smooth sidewall profile. For VCSEL fabrication, the ICP tool is used to etch through the top DBR layers and the intrinsic MQW active region. The etching is controlled to stop on the n-DBR stack for placing the n-type contact metal. Also, the $Al_{0.98}Ga_{0.02}As$ layers need to be exposed properly for better control of the oxidation process.

For this high speed VCSEL material, because of the AlAs layers in the n-DBR, the ICP etching control is critical to prevent those layers from being exposed and oxidized and causing low yields. The oxidation rate of AlGaAs layers has an approximately exponential dependence on the Al-composition. Thus, lateral oxidation of the AlAs layers with the oxidation time calibrated for the $Al_{0.98}Ga_{0.02}As$ aperture layers may cause blocking of the electron injection from metal contact into the active region and also affect the heat transportation out of the active region negatively. We use a laser interferometry apparatus to monitor the ICP etching. Because of the change of reflectance off the sample surface as etching though the high/low index AlGaAs layers, we can use the periodic variation of the surface reflectance to monitor the ICP etching. However, the etch rates in the bulk area and around the mesas are different. The laser beam is focused onto the bulk area, so one of the important parameters during the development of process is to know the difference of the etching in the bulk area and around the mesas, and usually the difference is about 3 to 4 pairs of DBR. Previously, for our 40 Gb/s VCSELs [5], this difference can be dealt with by simply etching 4 to 6 more pairs of the n-DBR after interferometry shows the intrinsic active region is etched. However, below the active region, there are only 3 pairs of $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$ in this material's bottom DBR, so the number of pairs we can overetch is limited.

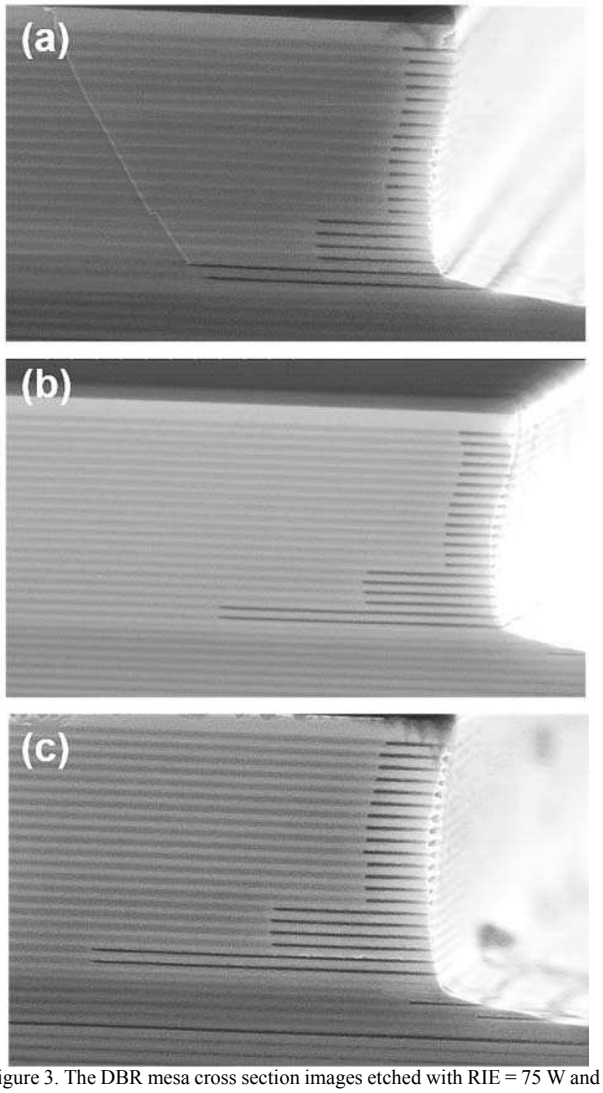

Figure 3. The DBR mesa cross section images etched with RIE = 75 W and ICP = 100 W. In (a), the $Al_{0.98}Ga_{0.02}As$ layers are oxidized unevenly because the bottom one sits on the etch foot. Two more pairs of n-DBR are etched in the bulk area for (b). The 2 $Al_{0.98}Ga_{0.02}As$ layers are oxidized evenly. One additional pair is etched for (c), and an AlAs layer is exposed and oxidized.

Figure 2 (a) shows a SEM cross section of an intentionally overetched DBR mesa with several AlAs layers in the bottom DBR exposed, and the darker lines are the oxidized part. The oxidation of the AlAs layers goes much deeper into the mesa compared to the oxidation of the aperture $Al_{0.98}Ga_{0.02}As$ layers.

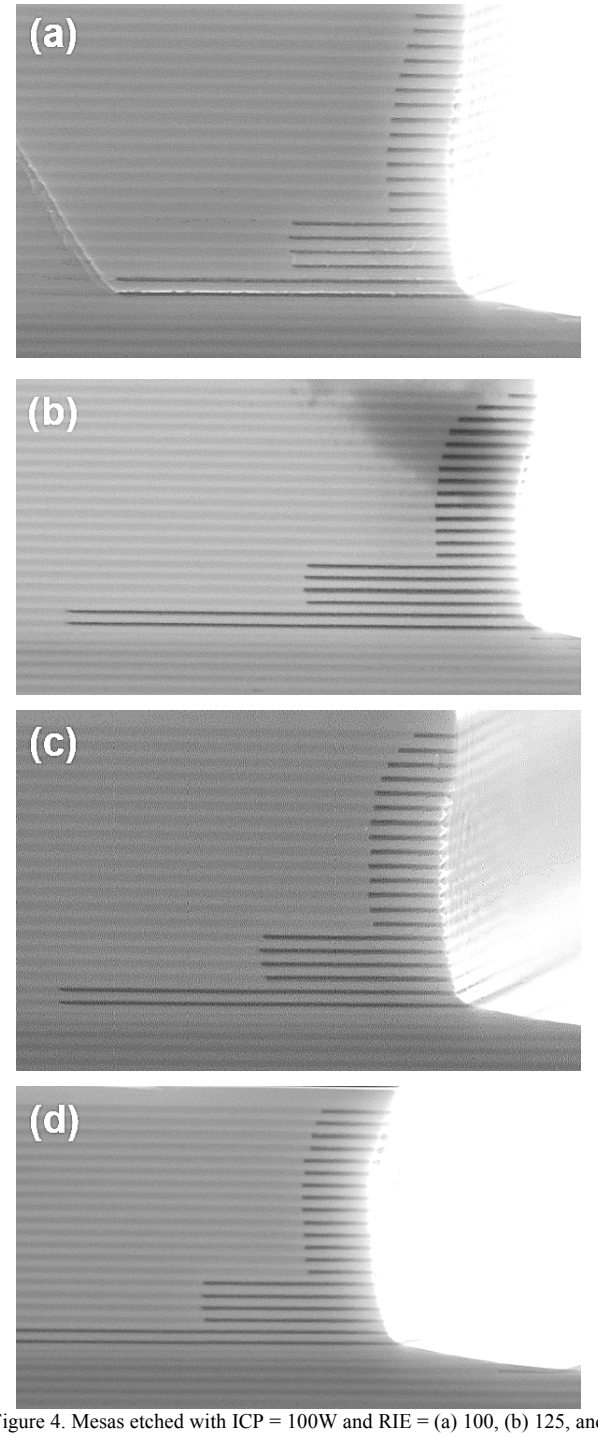

Figure 4. Mesas etched with ICP = 100W and RIE = (a) 100, (b) 125, and (c) 150 W with the same amount of overetch. The $SiCl_4$ is doubled from 2 to 4 sccm for (d) and RIE = ICP = 100 W.

Figure 3 (a), (b), and (c) are the cross section SEM images of 3 DBR mesas etched with the same pressure, etchant gas combination, and RIE, or the platen RF power, = 75 W and ICP = 100 W power setting but with different number of pairs of DBR overetched. From the SEM images, the etching profile around the foot of the mesa shows a slope-like transition which called the etch foot. In Figure 3 (a), although the etching has passed the intrinsic region, one of the $Al_{0.98}Ga_{0.02}As$ layers sits on the etch foot, and this causes the 2 $Al_{0.98}Ga_{0.02}As$ aperture layers to oxidize unevenly. We etch 2 more pairs of the n-DBR for the mesa shown in Figure 3 (b). The bottom $Al_{0.98}Ga_{0.02}As$ layer now does not sit on the etch foot, and the 2 aperture layers are oxidized evenly. In Figure 3 (c), 1 more pair of n-DBR is etched, and the AlAs layer in the bottom DBR is exposed. The oxidation of the AlAs is much faster than the $Al_{0.98}Ga_{0.02}As$ layers, and this should be avoided during the process.

We further test various RIE power settings with the same amount of overetch. Figure 4 (a) to (c) show the cross section of DBR mesas etched with different RIE power: (a) 100, (b) 125, and (c) 150 W. In the vertical direction, all the etching conditions are able to expose the aperture layers properly but not the AlAs layers. The difference between the etching profiles lies in the lateral direction. With higher RIE power, the mesas are etched more in the lateral direction, but the difference is not drastic. We also test the etching with different etchant gas composition. The mesa in Figure 4 (d) is etched with an increased $SiCl_4$ flow from 2 to 4 sccm as compared to the other test etchings in Figure 4 (a) to (c). The RIE and ICP power are both set to 100 W, same as in Figure 4 (a). Although the vertical etching is similar, there is more etching in the lateral direction. Eventually, we choose the etching recipe used in Figure 4 (a) considering the etching rate, the etching profile, and the control of the process. Figure 5 shows a SEM cross section of a fabricated device prepared by focused ion beam (FIB). The $Al_{0.98}Ga_{0.02}As$ are oxidized evenly, and the AlAs layers in the n-DBR are not exposed.

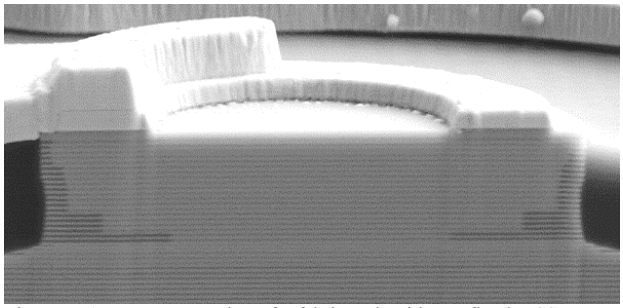
Figure 5. A FIB cross section of a fabricated oxide-confined VCSEL. No oxidation of the AlAs layers is observed.

DEVICE PERFORMANCE

The VCSEL device shows a threshold current of 0.8 mA at 25 °C, and from the mode spacing of its optical spectrum, the estimated optical modal diameter (d_0) is ~5 μm. Figure 6 (a) shows the optical frequency response of the VCSEL. The device shows a high modulation bandwidth of 29.15 GHz. We then perform the eye diagram and bit-error rate (BER) measurement to test the device's ability to transmit

high speed data. The BER vs. received optical power in Figure 6 (b) shows the BER measurement at 57 Gb/s data rate with a non-return-to-zero (NRZ) 2^7-1 bit length pseudorandom binary series (PRBS7) bit sequence and V_{PP} = 0.65 V. The inset shows the eye diagram at 57 Gb/s, and the device is able to show open eye at the data rate. For directly modulated 850 nm oxide-confined VCSELs, 57 Gb/s is the highest error-free data rate to date without using external equalizers to improve the BER [8].

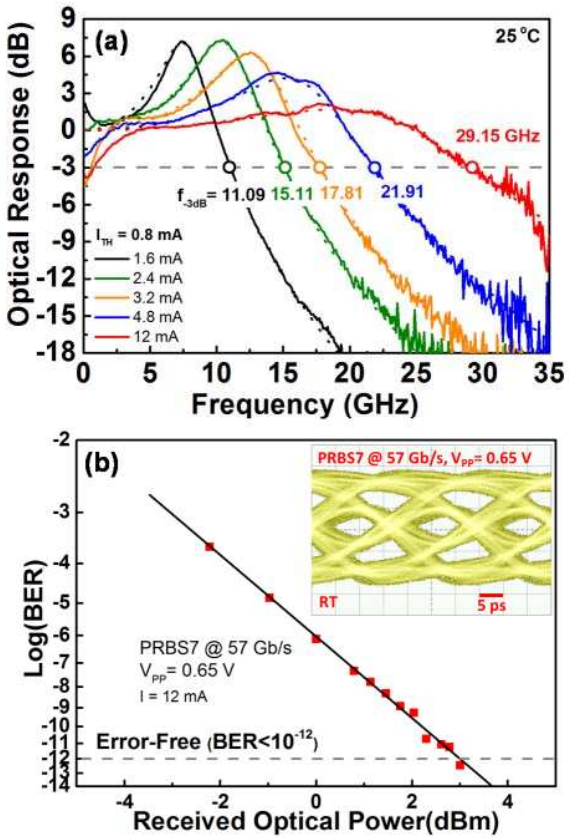

Figure 6. (a) The optical frequency response of the VCSEL device at 25 °C. The highest bandwidth is 29.15 GHz measured at 12 mA bias. (b) The BER vs. received optical power at 57 Gb/s data rate. The inset shows the 57 Gb/s eye diagram.

CONCLUSION

For better heat transfer out of the active region while operating under high bias current, the VCSEL material includes binary AlAs layers in the bottom n-DBR for their higher thermal conductivity. We develop the ICP etching process for the top DBR mesa etching to expose the aperture $Al_{0.98}Ga_{0.02}As$ layers properly for uniform oxidation depth but not the AlAs layers in the bottom n-DBR. The fabricated device shows a high modulation bandwidth of 29.15 GHz and is able to demonstrate 57 Gb/s error-free data transmission.

ACKNOWLEDGEMENTS

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ACRONYMS

VCSEL: Vertical Cavity Surface Emitting Laser
ICP: Inductively Coupled Plasma
RIE: Reactive Ion Etching
DBR: Distributed Bragg Reflector
BCB: Benzocyclobutene