# Ablation Laser Dicing for GaN HEMT Device on 100µm SiC/Au Substrates

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**Abstract**

**A laser dicing process has been developed for the Qorvo's GaN MMIC process flow to replace mechanical sawing. It improves fab cycle time, decreases the saw street width, increases the number of die per wafer, and reduces cost. Qorvo has qualified laser dicing for all of its GaN MMIC production flows with comparable visual and assembly yields. This report describes the laser dicing process development in detail.**

## INTRODUCTION

GaN HEMT devices are very attractive for commercial and defense applications, ranging from L-band to W-band, due to their high breakdown voltage, high frequency, and high power capabilities. Qorvo Inc. is one of the industry leading companies in GaN HEMT technology development and has achieved DoD Manufacturing Readiness Level 9 (MRL9) for 0.25µm GaN HEMT technology. Subsequently, the 0.15µm and 0.5µm GaN technologies have also been released to production.

Due to high wafer cost of the SiC substrate and GaN epi growth it is critical to maximize the number of die per wafer to reduce the production cost per die. An effective way to maximize the usable chip area on a wafer is to reduce the saw street width. Mechanical sawing with abrasive diamond blades is generally used to dice GaN devices on SiC substrates. The main problems with mechanical sawing is that it is a slow process and the diamond saw blade rapidly wears out since SiC has a hardness which is 96% of that of diamond. Saw blades also tend to meander during sawing resulting in die chipping and a large kerf width. Therefore, the street width for mechanical sawing has to be wide enough to accommodate the backside chipping and blade drift.

Laser dicing has been used for years and is accepted as a common method to dice Si and GaAs wafers but is not as widely used for SiC wafers. In this paper, the authors describe the development of a laser saw process for 100µm thick SiC substrates which is used in all of Qorvo's GaN HEMT technologies. The laser saw process lowers production cost, reduces cycle time, and more importantly creates more usable die area and increases the die count per wafer. In addition, the final die dimensions are much more precise and repeatable allowing tighter assembly tolerances and improved die on tab RF performance.

## EXPERIMENT

GaN on SiC laser dicing development was performed with an IR ablation laser saw tool. It uses short laser pulses to heat the SiC until it melts or vaporizes with no physical contact. The result is high quality and high speed cutting through thin compound devices and metals. The street can be greatly reduced by focusing the laser beam to a spot less than 10µm.

Several challenges were encountered in developing the laser dicing process. First, laser dicing through a 100µm SiC substrate generates slag and recast along the kerf as shown in Figure 1. The slag and recast can cause visual and assembly yield loss. Second, the laser beam can create a heat-affected zone in the SiC with a peak temperature of 2750 °C. Such a high temperature zone could potentially degrade nearby GaN devices. Third, slag and recast can also accumulate between the wafer backside and mounting tape causing assembly solder voids and yield loss.

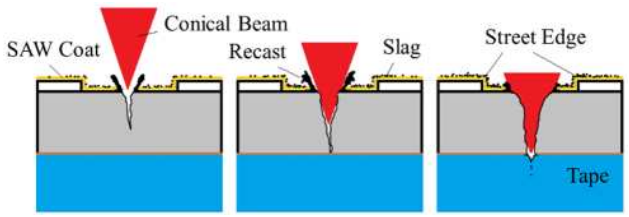



Figure 1. Ablation laser dicing process.

Extensive DOEs were conducted with various process factors to define the optimal process settings to minimize the laser saw recast range. A thermal model was also developed and verified experimentally to map out the safe temperature zone (< 250 °C) for device placement. The wafer backside process was also optimized to prevent backside recast buildup. Optimized design rules of street-to-metal pad distance were then verified on development lots with various street widths and confirmed on production lots. Visual and assembly yield, and RF performance were compared between laser saw and mechanical saw, on dies from the same wafer showing comparable results.

RESULTS

Slag and Recast Reduction

Multiple design of experiments were conducted to define the optimal process parameters with minimum slag and recast range. The key parameters that impact the edge recast range are stage speed, laser power, number of laser passes, laser beam trigger step/pulse frequency, and laser focus offset. Recast size vs. dicing speed is shown in Figure 2, which shows lower dicing speed results in lower recast range. High dicing speed tends to cause considerable amount of subsurface fracturing as shown in Figure 3. Laser pulse frequency limits the possible trigger step distance. The trigger step is the distance a wafer travels between firing the laser. Figure 4 showed the trigger step of 1st pass is a bigger factor than second pass trigger step in terms of through-cut. Figure 5 showed the high laser power or dose is needed to cut through SiC substrate. Kerf and recast wall width can be manipulated significantly by varying beam focus. Positive focus offsets following the first pass tends to have a "cleaning effect" on the near-kerf recast sidewall resulting in wider and shallower cuts. Stepping focus offsets below surface after the first pass however, removed topside recast and increased overall cut depth.

Based on the DOE results, a three pass laser dicing process was chosen which through cut the SiC substrate and coated Au metals with minimum recast and no subsurface fracturing. The final street image post laser dicing is shown in Figure 6.

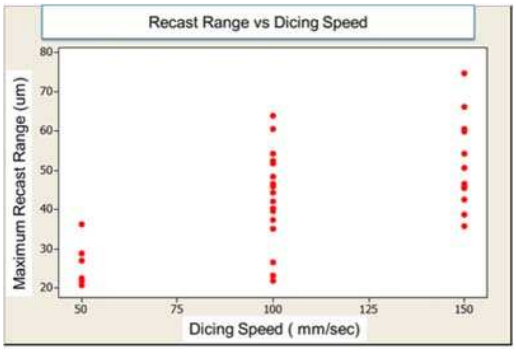



Figure 2. Recast range vs laser dicing Speed.

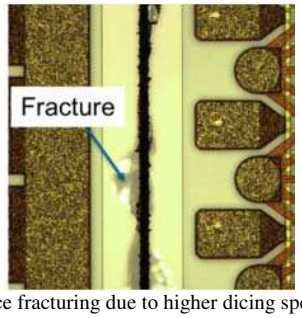
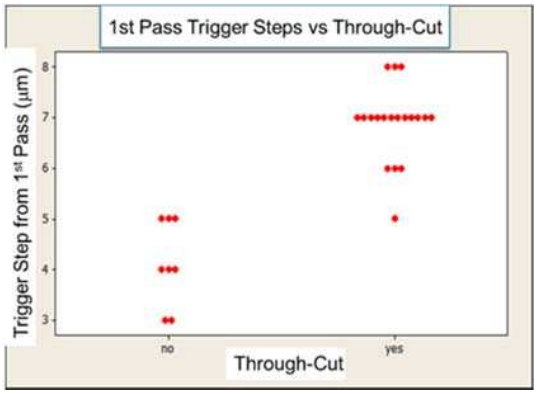
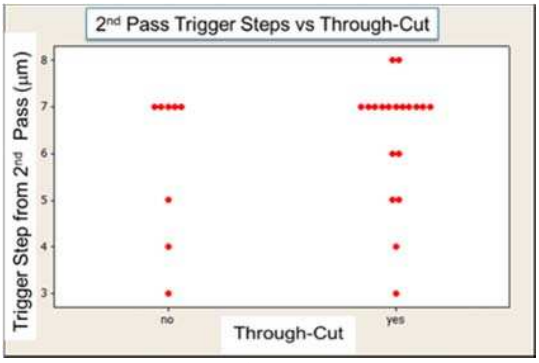



Figure 3. Subsurface fracturing due to higher dicing speed.




(a)




(b)

Figure 4. Trigger step vs. through cut for first pass cut (a) and second pass cut (b).

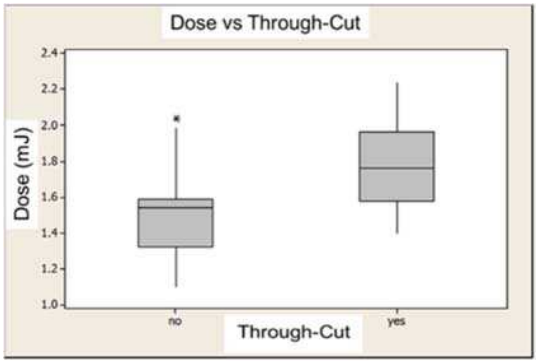



Figure 5. Laser pulse dose vs. through cut.

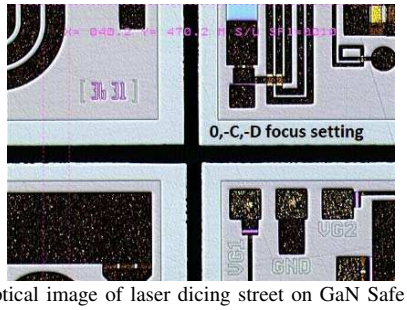



Figure 6. Optical image of laser dicing street on GaN Safe Temperature Range

Thermal models for laser dicing through Si, glass, GaAs and sapphire are available commercially. However, it is difficult to find the thermal model for laser saw cutting through SiC substrate. In order to minimize the GaN die size it is necessary to shrink the street size and place the devices as close as possible to the street. Due to the excellent thermal conductivity of SiC substrate, the temperature from the center of the peak temperature of 2750 °C will drop very quickly.

Several experiments were conducted using proprietary method with laser dicing through SiC wafers. Figure 7 shows the extrapolated temperature vs. normalized distance from the cut center. From this curve one can define the proper distance for GaN HEMT device placement to prevent thermal shock or stress (<250 °C). This distance is 65% shorter than that required by mechanical saw which is determined by die chipping.

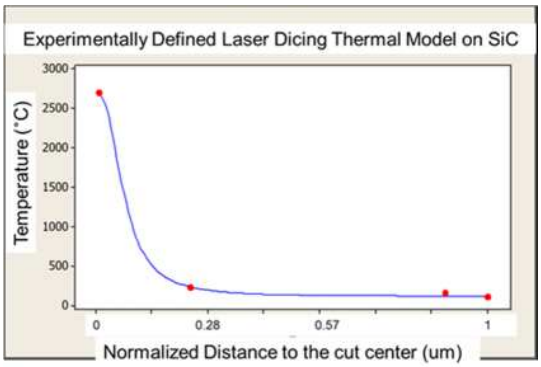



Figure 7. Experimentally defined temperature during laser dicing as a function of the distance from the center of the dicing street.

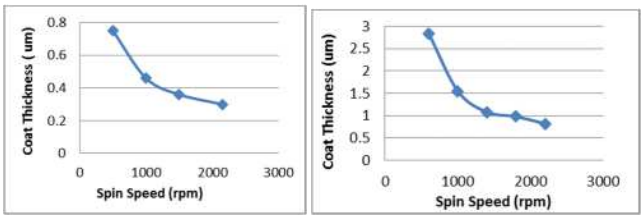
## Saw Coat Evaluation

To protect the device surface from slag/recast, two types of spin-on coating were evaluated. The first type was chosen based on its compatibility with an existing mechanical dicing process. Although this option would have been the most convenient, the non-water soluble coating was neither resilient nor thick enough even at the slowest possible spin speeds (500rpm) to withstand falling slag, particularly along the outer-most edges of tall topography where the coating was thinnest. The second water-soluble PVA-based coating, which was actually intended for laser dicing applications, coated thicker than the first and provided better protection at all spin speeds tested. Coat thickness as a function of spin speed for both types of coating is shown in Figure 8.

Regarding tall topography coverage and recast wall width, spin speed was found to be the primary factor. For isolated coat blowout defects, cure time and wafer positioning were most critical. Process was optimized to minimize yield loss due to post clean slag/recast-related defects.

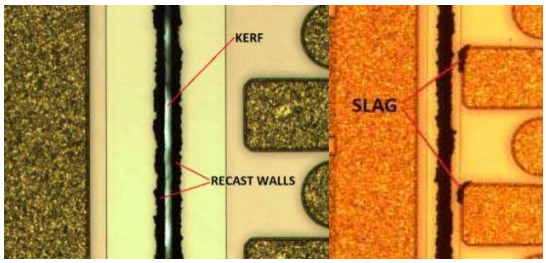
It was observed that while slower speeds yielded a thicker coat and thus better protection on tall topography, the resulting recast wall on both sides of the kerf was wider than desired ( recast wall widths of 80% of the entire dicing street) as shown in Figure 9 (a). At higher spin speeds, the recast wall width was narrower and overall more consistent, but the outer-most edges of tall topography were not adequately protected from slag. After coating removal, clumps of slag remained stuck to structures nearest the kerf as shown in Figure 9 (b). Optimal spin coating was determined to provide both acceptable recast wall width and sufficient protection for near-kerf topography.

Coat curing conditions were also scrutinized and controlled (including oven temperature, cure time, wafer orientation, cassette spacing, etc.) to eliminate wafer to wafer and within wafer variations in coat coverage. If the PVA coat is not cured adequately, pockets of trapped solvent expand and explode during laser dicing resulting in un-protected areas and subsequently coat blowout defects as shown in Figure 10. If instead the PVA coat is over-cured, it can prove difficult to remove once laser dicing is complete.




(a) (b)

Figure 8. Coat thickness as a function of spin speed for the first type of coat (a) and the second type (b).




(a) (b)

Figure 9. Optical images of laser dicing street and defects. (a) With slow coat speed; (b) with high coat speed.

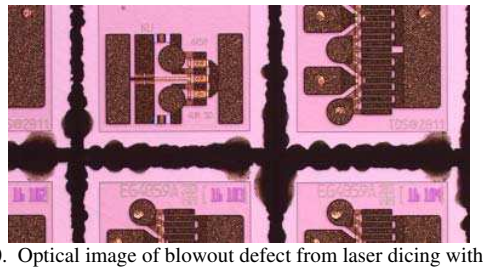


Figure 10. Optical image of blowout defect from laser dicing with coat in-adequately cured.

In addition, first & last wafer effects (regarding slot positions in cassette during cure) were also observed, which were mitigated by bookending production material with pilot

substrates. Even spacing between wafers as well as vertical positioning proved to be contributing factors in minimizing the appearance of isolated blowout defects.

## Device and Assembly Evaluation

After the laser saw process was defined a DOE mask was designed with various saw street sizes and various distances of device placement to the center of the street. Visual yield was collected as seen in Table 1. The visual yield results demonstrated the minimum distance that GaN device can be placed without recast on the metal pads.

GaN FET reliability data is collected to confirm no thermal and mechanical stress from laser dicing. As shown in Figure 11, median lifetimes (t50) at 95% confidence are not significantly different between mechanical saw and laser dicing. In addition, RF testing of the laser cut die and mechanical cut die from the same wafer also showed the same performance and no device performance degradation from thermal or mechanical stress.

Table 1. Visual yield on DOE mask with various street size and device to street size. X indicated recast is seen. 0 indicated no recast is observed on wafer surface.

| | | Condition A | Condition B |
|---|---|---|---|
| Total Street Size (um) | Center of street to Metal Pad (um) | % dies with recast on metal pads | % dies with recast on metal pads |
| 80 | 65 | 0 | 0 |
| 70 | 60 | 0 | 0 |
| 60 | 55 | 0 | 0 |
| 70 | 60 | 0 | 0 |
| 70 | 55 | 0.66 | 0 |
| 70 | 50 | 2.63 | 0 |
| 70 | 35 | 41.4 | X |
| 70 | 35 | 25.7 | 0 |
| 70 | 45 | 4.61 | 0 |
| 70 | 40 | 3.95 | 0 |
| 80 | 40 | 28.9 | X |
| 80 | 45 | 1.97 | 0 |

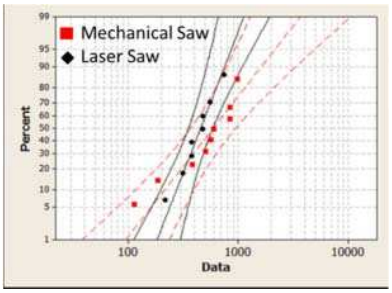
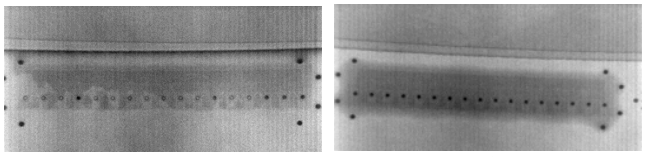



Figure 11. Probability plot of FET DC lifetime comparing mechanical saw and laser saw.

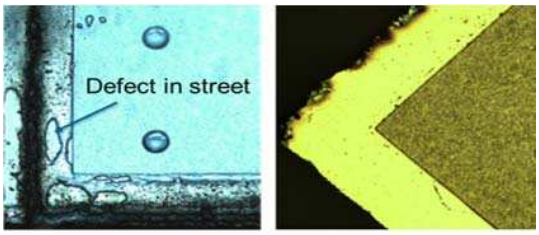
Laser sawn dies were also assembled in packages using standard solder process, then x-rayed to check for solder voids. Initial tests showed a 16% yield loss due to solder voids as shown in Figure 12(a). This was due to recast piling up in the backside metal street between the wafer and the mounting tape and blocking the solder flow.



(a) (b)

Figure 12. X-ray images on assembled die from laser saw process. (a) Solder voids (white spots) are apparent from initial laser saw process. (b) No solder voids are seen from final laser saw process.

Figure 13 shows the street defect from two different mounting tapes. Strong adhesion tape helped prevent recast slip under the tape. After implementing a new backside metal process with stronger mounting tape, the x-ray yield increased to 98.5% as shown in Figure 12 (b) which is comparable to the baseline mechanical saw yield. Die from laser dicing has also gone through 1000 thermal cycles without failure.




(a) (b)

Figure 13. Optical images of street defects from mild adhesion tape (a) vs strong adhesion tape (b)

## SUMMARY

A laser dicing process was developed and released for all of Qorvo's GaN production flows. The laser dicing process was free of backside chipping, lowered production costs, improved cycle time for die separation by 95%, and increased die per wafer for 20 mm discrete GaN FETs by 32% over mechanical saw. Laser dicing also reduced the kerf width by 75% with a 92% improvement in kerf centering accuracy. Moreover, it helps MMIC module and die on tab performance with tighter assembly tolerances and shorter wire bonds which reduce packaged inductance.

## ACKNOWLEDGEMENTS

The authors would like to thank Qorvo colleagues who contributed to the measurements and wafer processing.

## ACRONYMS

PVA: Poly Vinyl Alcohol
DOE: Design of Experiment