

Temporary Bonding for Backside Processing of 150-mm SiC Wafers

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Abstract

In this paper, we present a cost-efficient wafer support system for thin wafer handling of silicon carbide (SiC) device wafers by using a low-stress temporary bonding material and a glass carrier with a coefficient of thermal expansion (CTE) matched to that of a SiC wafer in place of a traditional sapphire or SiC carrier. The ability of the glass manufacturer to adjust the CTE of a glass carrier to match that of the different device substrates is one of the key factors that allow implementation of glass carriers for thin wafer handling has several advantages. Here, we present some of the key elements for showcasing the compatibility of glass carriers with III-V device manufacturing, including a comparison of CTE-matched glass across the different III-V semiconductor substrates, the ability of the glass to survive various backside processes that are encountered in compound semiconductor device manufacturing, and the compatibility of glass wafers with an array of debonding methods.

INTRODUCTION

A variety of device substrates are encountered during manufacturing of compound semiconductor devices, including SiC, gallium arsenide, gallium nitride, indium phosphide, and other substrates. The wafer sizes also vary greatly from 2-inch to 200-mm substrates depending on the manufacturing capabilities and economics of the process. More recently, 150-mm device manufacturing has been widely adopted, and as demand for these devices continues to grow, 200-mm wafers are being considered as a means to realize economies of scale. During the fabrication of the devices, most of these wafers encounter wafer-thinning processes to reduce the device wafer thickness for better heat dissipation and to enhance device performance. The wafers are often thinned to much less than 100 μm , and the thinned substrates frequently have high topography and are very fragile at these low thicknesses. Thus, a temporary wafer support system becomes essential to handle these fragile substrates. The temporary bonding system and the thin wafer handling technology must be capable of supporting the device from the initial wafer-thinning step through various backside processes and finally all the way to the debonding step while providing a simple, cost-efficient, and high-yield process. It

is important for the wafer support system, which includes the bonding material and the temporary carrier, to apply the lowest possible amount of stress to the device wafer throughout the process. The bonding materials used here are engineered for very low stress, and the glass carriers have their CTEs matched to the device wafer to avoid undue stress on the device wafer. We also employ glass carriers of various thicknesses to understand the effects of thickness on process stability and thermal conductivity.

BACKGROUND

Brewer Science has been working with a customer to implement a thin wafer handling technology using a wafer carrier that allows for low cost of ownership and to add more stability to the wafer by means of reducing the total bow encountered by the bonded stack during backside processing. Reduction in bow is critical to enabling the use of larger substrates for device manufacturing, as bowed wafers are difficult for fab equipment to handle and often contribute to yield loss.

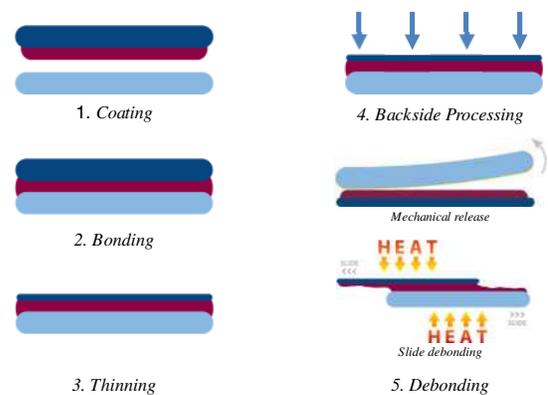


Figure 1. Simplified schematic representation of temporary bonding and thin wafer handling

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Figure 1 above shows a simplified schematic of the temporary bonding and thin wafer handling process in the compound semiconductor fabrication process. The device wafer is bonded to a carrier wafer using a bonding material layer. Then after grinding and other downstream processes, the device wafer is separated from the carrier wafer using a specific debonding method. The use of CTE-matched glass as a carrier wafer provides many advantages in wafer processing applications. The transparent substrate provides an opportunity for facile optical and visual inspection of bond line for voids, bubbles, or other defects after bonding and before downstream processing. This simple, low-cost inspection avoids the use of expensive and time-intensive confocal scanning acoustic microscopy (CSAM) methods for inspecting the integrity of bond lines, thereby increasing the overall throughput of the process. Moreover, glass has good chemical resistance in harsh chemical environments, so the carrier wafers can be reused for temporary bonding applications multiple times, thereby lowering the cost of the process. More importantly, the glass manufacturer can adjust CTE of the carrier by adjusting the glass composition, thereby allowing minimal bow and warp of the bonded pair. In this experiment, we used Corning® Eagle XG® glass.

EXPERIMENTAL

An experiment was constructed to assess the performance of glass carriers for SiC wafer processing. Two debonding methods were evaluated, a room temperature mechanical debonding method and a slide debonding method. The device wafers used were 150-mm bare SiC wafers, and the bonding material used for this study was BrewerBOND® 220 material, a thermoplastic bonding material with excellent chemical resistance, thermomechanical stability, and melt flow viscosity that is conducive for high-temperature processing up to 200°C and is suitable for thermal slide debonding. For the room temperature mechanical debonding process, BrewerBOND® 510 material was used as a release layer. The release layer was coated and baked on the glass carrier wafers, which were then bonded to SiC wafers coated with BrewerBOND® 220 material. Figure 2 shows the schematic of the wafer coating setup for slide debonding and the mechanical release method of debonding.

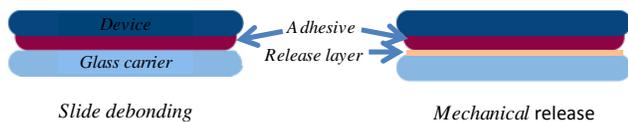


Figure 2. Schematic of wafer coating setup for slide debonding and mechanical release debonding

For using the slide debonding method, the bonding material layer bonds to the SiC wafer and carrier wafer directly, whereas for mechanical release debonding, a release

layer is used on the carrier wafer to enable easy debonding while adhering strongly enough for the wafer pair to remain bonded through the entire backside processing steps and wafer grinding process. A PosiTest AT adhesion tester was used to measure adhesion strength of the bonding material with and without the release layer. This test method and equipment conforms to international standards including ASTM methods D4541, D7234, and ISO4624. The method uses a vertical pull test to measure the adhesion strength of the bonding materials to the wafer. Samples were generated using the BrewerBOND® 220 bonding material and BrewerBOND® 510 release layer material on test wafers using standard coating and baking conditions. Then standard operating procedures were followed to pull the wafers apart using the PosiTest adhesion tester. Table I shows the adhesion strength of bonding materials used in slide debonding and mechanical release methods. From the data, it can be seen that the adhesion strength of BrewerBOND® 220 material with release layer is 6.5 psi, and the adhesion strength without the release layer is ~3 times more, 17 psi.

TABLE I
ADHESION STRENGTH OF BONDING MATERIALS

Bonding Materials	Adhesion strength (psi)	Std. deviation (psi)
BrewerBOND® 220 (for slide debonding)	17	1.8
BrewerBOND® 220 with release layer BrewerBOND® 510 (for mechanical release)	6.5	0.6

Once the SiC wafer is bonded to a carrier wafer using the bonding material, the bonded stack has a residual bow. Subsequent processes such as backgrinding, CVD, ICP dry etching, and other process also further contribute to the bow and warp of the bonded stack. We compared the amount of bow in a bonded stack with CTE-matched glass carriers to traditional sapphire carriers on SiC substrates. One of the important factors that affect the bow of the bonded stack is the CTE of carrier.

TABLE II
COMPARISON OF CTE FOR VARIOUS WAFER TYPES

Substrate	CTE (ppm/°C)
Glass carrier	3.2
Sapphire carrier	5.3
SiC wafer	4.0

Table II shows the CTEs of silicon carbide substrates, sapphire, and CTE-matched glass carriers. Sapphire carriers have a high thermal conductivity, which is helpful to dissipate the heat away from the device wafer in the bonded stack during backside processes with a high thermal load. Thermal dissipation is important to prevent delamination and

excessive bow or warp of the thinned device wafer during backside processing, which can result in wafer breakage or non-uniformity in the subsequent processing steps. However, sapphire carriers have a high CTE mismatch with the device wafer. At wafer sizes less than 100 mm, the CTE mismatch does not have a large impact on the device wafer, but at larger substrate sizes, the CTE mismatch between the sapphire carrier and device wafer becomes a dominant factor that causes an increase in the bow of the bonded stack such that it cannot be processed further. Table III compares the bow measurements of CTE-matched glass carriers to sapphire carriers using different thicknesses of BrewerBOND® 220 bonding material. It can be seen from the table that, for the same thickness of the bonding material, bonded stacks with the CTE-matched glass carriers result in much lower bow compared to the sapphire carrier under similar conditions. The bow and stress effect becomes more pronounced as the wafer sizes increase.

TABLE III
BOW COMPARISON OF GLASS AND SAPPHIRE CARRIERS USING BREWERBOND® 220 BONDING MATERIAL

Film thickness bonding material (µm)	Bow using 0.7-mm-thick CTE-matched glass carrier (µm)	Bow using 1.1-mm-thick sapphire carrier (µm)
30	50	225
40	50	175
50	40	125

In the first baseline study, all backside processing was completed on bare SiC wafers using a sapphire wafer as a carrier. The bonding material was coated at various bond line thicknesses: 30 µm, 40 µm, and 50 µm. After bonding the SiC wafer to the sapphire carrier wafer, the wafer underwent various backside processing steps from grinding to metal evaporation, etch, and photolithography. The bow of the bonded stack was measured at every step of the backside process.

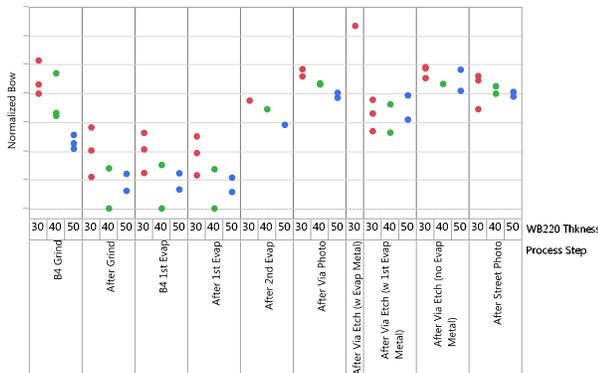


Figure 3. Bow measurement of bonded stack with sapphire carrier after each processing step and using various bonding material thicknesses

In this study, it was found that the lowest bonding material thickness, 30 µm, caused more bow and delamination during the backside processing. The 50-µm coating thickness had significantly lower bow across all the process steps, and no delamination was observed on the process wafers after completing all the downstream processing. Thus, for the next stage of experiments using CTE-matched glass carriers, 50 µm was chosen as the optimal bond line thickness for the BrewerBOND®220 temporary bonding material.

For the next experiment with CTE-matched glass carriers, we considered 3 thicknesses of glass wafers – 0.5 mm, 0.7 mm, and 1.1 mm. Multiple thicknesses were chosen to address the reduced thermal conductivity of glass carriers compared to sapphire carriers, and then an optimal carrier thickness was chosen based on the results from the backside processes. The 0.5-mm glass carriers were the thinnest carriers that could be obtained commercially.

The experiment was split to handle both mechanical release and thermal slide debonding methods. The wafers were coated with BrewerBOND® 220 material at 50-µm bond line thickness, and a few selected carrier wafers were coated with BrewerBOND® 510 release layer material to enable mechanical debonding. Then the bare SiC device wafers were bonded to CTE-matched glass carriers using standard process methods. The bonded wafer pairs that used the 0.5-mm glass carrier delaminated early on during handling of the wafer pairs after the bonding step most likely due to the flexibility of the thin glass wafer. As a result, the 0.5-mm glass wafers were not further included in this study. The wafer pairs bonded using a 0.7-mm glass carrier and a 1.1-mm glass carrier were subjected to further downstream processing steps that included backgrinding, metal evaporation, ICP dry etch, and photolithography. The bow of the bonded stack was measured after every step of the backside process.

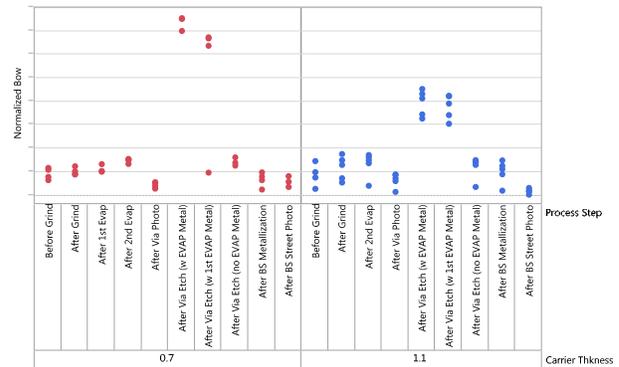


Figure 4. Bow measurement of bonded stack with 0.7- and 1.1-mm glass carrier wafers after each backside processing step

Figure 4 shows the comparison of the bow of bonded wafer pairs with the different thicknesses of glass carriers

after each step of the backside process. As seen from the data, the bow distribution at each process step for various wafers is grouped more tightly while using glass carriers with the 0.7-mm thick glass carrier having a tighter grouping than the 1.1-mm carrier. All the wafers survived the backside processing steps, proving that CTE-matched glass carriers can be as effective as sapphire carriers for 150-mm SiC wafer processing. Subsequent to the backside processing, the respective wafers were debonded using mechanical and slide debonding methods.

CONCLUSIONS

From the experimental results and data, it can be seen that CTE-matched glass carriers could be effectively substituted for sapphire carriers for supporting thin SiC wafers during backside processing for compound semiconductor device manufacturing. These glass carriers together with the BrewerBOND® 220 material allow for uniform expansion of both the carrier and the device during the various backside processes without causing undue stresses on the bonded wafer stack. No issues related to thermal conductivity were encountered during the process while using the 0.7- and 1.1-mm-thick glass carriers. A 50- μm thick coating of the bonding material in the bond line offered optimal performance. Moreover, the wafer bow data showed that the BrewerBOND® 220 bonding material with the CTE-matched glass allows for lower bow of the bonded stack during all backside processing when compared to the sapphire carriers. These results show a path for developing a cost-effective wafer support system using CTE-matched glass carriers for compound semiconductor manufacturing.

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ACRONYMS

CTE – Coefficient of Thermal Expansion

CSAM – Confocal Scanning Acoustic Microscopy