GaN on Diamond: Pushing the Boundary of Conventional MMIC Design and Fabrication

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Keywords: GaN, Diamond, ICECool

Abstract

This paper discusses the ongoing results of Raytheon's work on the Intrachip/Interchip Enhanced Cooling (ICECool) effort under contract with DARPA. The goal of this work is to enhance the performance of RF power amplifiers through the application of chip-level heat removal by intra- and/or interchip microfluidic cooling. This paper gives specific attention to developments and challenges in MMIC design and wafer manufacturing now that improvements in thermal management permit more aggressive electrical performance.

INTRODUCTION

As GaN device technology matures into production it has become clear that while GaN-based transistors are capable of higher power density, their true performance potential is limited by thermal impediments [1]. We are researching a high-performance thermal management strategy that replaces the native growth substrate of GaN epi with a high-conductivity CVD diamond substrate for enhanced heat spreading, and then followed by inclusion of microchannels within the diamond substrate for convective heat removal. This thermal improvement unlocks a key barrier to pushing GaN higher in performance, with the potential to become the next revolution in III/V semiconductors [2-3]. We describe the results of a program funded by DARPA to increase the power handling capability of today's state of the art GaN by as much as 5X. This paper focuses on the implications of this technology from an electrical and manufacturing perspective rather than from a thermal perspective, which has been published previously [4].

MATERIAL

Wafers used on this program were created by Element 6, the industry leader in GaN on Diamond wafers. To make the GaN on Diamond wafers, GaN was lifted from commercially available GaN on Silicon wafers and the growth Silicon substrate was replaced by directly-grown CVD diamond (Figure 1) [5]. In order to maximize thermal performance, the diamond substrate thickness was increased from 100um to nearly 350um. This additional thickness enables inclusion of microchannels in the diamond substrate. After wafer formation was complete, the wafers were then bonded to a temporary carrier wafer in order to be compatible with standard foundry equipment and then processed in Raytheon's III/V foundry. The electrical and material properties of CVD diamond as well as the carrier need to be considered during MMIC design and fabrication, and will be discussed in the next sections.

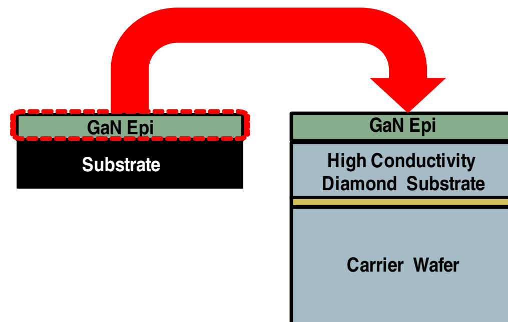

Figure 1: GaN epitaxial material is transferred from its growth substrate to a diamond substrate

DEMONSTRATION VEHICLE MMIC DESIGN

In order to highlight the enhanced thermal performance of GaN on Diamond and microchannel cooling, we designed a MMIC that operated at the same temperature as a baseline State of the Art wideband GaN on SiC MMIC, yet had a 5.0X increase in RF output power. This was accomplished through a 1.5X increase in bias voltage and 4.1X increase in final stage MMIC periphery (Table 1). In addition, we compacted gate-to-gate spacing within the transistor layout by 4.0X in order to accommodate the added periphery without increasing the size of the MMIC.

Table I
COMPARISON OF KEY PARAMETERS BETWEEN TODAYS MMIC AND ICECOOL DEMONSTRATIONMMIC

	ICECool compared to current State of the Art GaN/SiC
Substrate	**Diamond with microchannels**
Output Periphery	**4.1X increase**
Gate Pitch	**4.0X decrease**
Voltage	**1.5X increase**
Pout	**5.0X increase**

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The first step in converting the baseline design to a higher power version on the diamond substrate is to account for the differences in electrical properties between SiC and diamond substrates. Through measurement and modeling comparison of test structures fabricated on diamond wafers, we determined the diamond substrate exhibits an effective dielectric constant of 5.70, as compared to 10.03 for SiC. This means the same characteristic impedance transmission line on the same substrate thickness will need to be physically longer on diamond than on SiC to achieve the same electrical length. The second step includes co-design between thermal and electrical performance, which optimized the location of microchannels in the substrate simultaneously for maximum thermal (channel temperature) and electrical (transmission line insertion loss and consequently Power Added Efficiency) performance. The baseline design makes use of co-planar waveguide (CPW) transmission lines, which are formed on the substrate top surface by a center-line surrounded by two ground lines. The CPW line characteristic impedance is set by the widths of the center-line and the gaps between the center- and ground-lines.

We used ANSYS HFSS to investigate the impact of fluid-filled microchannels in the substrate on transmission line performance including optimizing the electrical placement of the microchannel (Figure 2). We first varied the clearance depth from the conductor surface to the top of the microchannel in the substrate from no channel to a depth of 80um (Figure 3, left). Results simulating a simple CPW transmission line showed that a clearance of only 5 um had a significant impact on insertion loss and impedance, while a depth of 80um negated the effect at our frequency range of interest, which is X-Band and below. Secondly, with clearance now set at 80um, we varied the location of the microchannel relative to the edge of the conductor surface, varying the lateral setback up to 50 um (Figure 3, right). Results showed that locating the microchannel underneath a conductive surface with any setback effectively negated any effect. With these results, we selected an approach that locates the microchannels with minimum clearance of 80um.

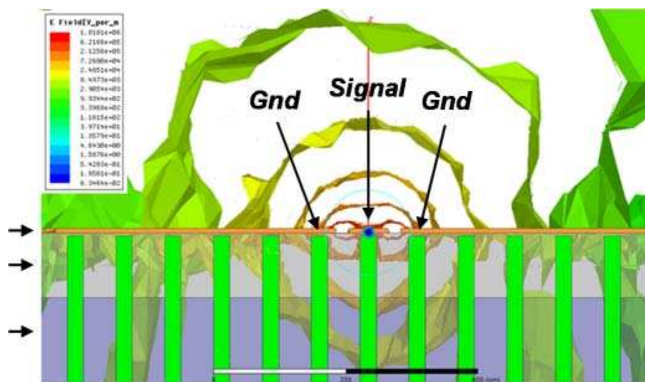

Figure 3: HFSS simulation of microchannel placement (green) underneath CPW transmission lines and ground place (orange) to reduce electrical impact.

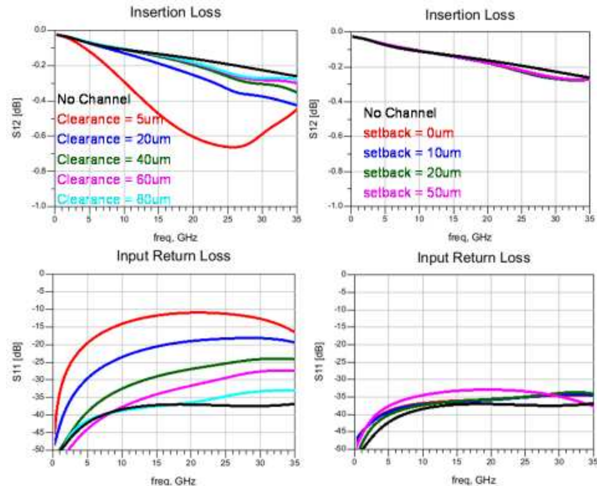

Figure 2: (left) HFSS simulation result of microchannel placement while varying depth underneath conductor surface, and (right) microchannel placement 80um below conductor while varying lateral setback from conductor edge.

GAN ON DIAMOND WAFER MANUFACTURING

Turning attention to wafer fabrication, GaN on Diamond wafers presently exhibit unique properties that require special consideration for processing in a standard semiconductor foundry. As the diamond substrates are grown at high temperatures while attached to a Silicon handle wafer, the dissimilar CTE properties of Silicon and Diamond (Figure 4) cause the GaN on Diamond wafers to bow upon cooling down to room temperature. Additionally, GaN on Diamond wafers are nominally thinner than commercially available III-V wafers due to the increased cost of growing diamond thicker, and are hence not compatible with the focal range of most production lithography machines. As a result, a supporting carrier wafer must be bonded to the underside of the GaN on Diamond wafer to reduce bow and add overall height.

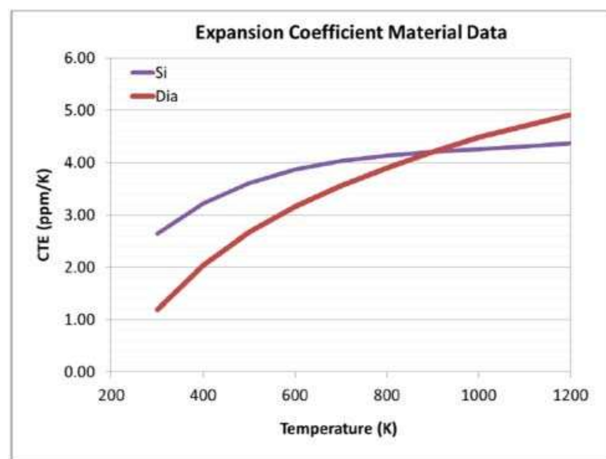

Figure 4: CTE of Silicon and Diamond. While matched near diamond growth temperatures, are mismatched at room temperature, causing wafer bow after diamond synthesis.

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While handle wafers and carrier wafers are not unique to semiconductor fabrication such as BEOL processing, they are unique for GaN on Diamond in that they are required for the entire fabrication sequence. The bond to the carrier must survive all foundry chemicals and a wide range of temperature excursions, yet also be removable after wafer fabrication is complete. Further, the carrier material must be stiff enough to reduce the bow of the GaN on Diamond wafer, and also be CTE matched to diamond to prevent unintentional demount at higher temperatures during the fabrication process. This criteria significantly narrows available bonding materials and carrier wafer possibilities. During this effort, we have identified a carrier material, bonding material, and developed a bonding process that permits GaN on Diamond wafers to be mounted in a manner than permits high-resolution lithography. This process is compatible with temperature excursions to 200°C, requiring demount and remount for any processing step with any temperatures higher such as nitride formation and ohmic alloying. So long as the flatness profile of the wafer to carrier mount can be maintained from mount to mount, each subsequent layer during wafer fabrication will be aligned to prior layers without impacting device yield.

After wafers complete front-side fabrication, backside processing commences, which typically includes formation of through-substrate vias to enable microstrip-mode MMICs. Processes and chemistries already existing for Silicon and SiC must be re-developed to create vias in diamond [6]. The chemistry for etching is unique and fabricating patterned features requires the use of novel masks that are not damaged or eroded during the diamond etching process. In addition, CVD diamond exhibits significant roughness not typically considered for in crystalline Silicon and SiC substrates, so special consideration must be given to the substrate preparation before via etching can commence. These unique processes for diamond have been developed, including a polishing and etch process that enables formation of vias in GaN on Diamond wafers (Figure 5). Further development is required to increase throughput, wafer size, and yield.

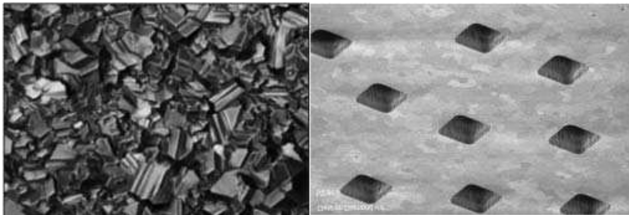

Figure 5: Diamond wafer backside surface before (left) and after (right) polishing and via formation

CONCLUSIONS

GaN on Diamond transistors have already been shown to offer 3x the thermal performance over production GaN on SiC [3], opening new opportunities for developing next-generation RF systems. New design practices accounting for diamond substrates and embedded microchannel cooling have been developed on this program to account for electrical and thermal co-design. New manufacturing practices required to process GaN on Diamond wafers addressing wafer bow, wafer thickness, backside roughness, and diamond etching have also been developed. The next phase of this program will utilize all of these tools, processes, and materials to manufacture GaN on Diamond MMICs, demonstrating the potential for GaN to operate at higher power densities, made possible by improved thermal management.

ACKNOWLEDGEMENTS

The authors thank Dr. Avram Bar-Cohen for his leadership of the DARPA ICECool and Near Junction Thermal Transport programs under which this work was performed. They also thank Dan Francis at Element 6 for assistance with carrier process development. This material is based upon work supported by the Defense Advanced Research Project Agency (DARPA) and United States Air Force under Contract No. FA8650-14-C-7469. The views expressed are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

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ACRONYMS

GaN: Gallium Nitride
CVD: Chemical Vapor Deposition
MMIC: Monolithic Microwave Integrated Circuit

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