Fabrication Process Induced ESD Damage of MIM Capacitors on a 0.15um pHEMT Process

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Abstract

This paper outlines the root cause analysis of a fabrication process-induced ESD damage on MIM capacitors in a pre-production pHEMT product. The average yield of the lot was only 70.2% during die sort. Of this, 17.5% of the lot failed due to improper pinching-off of the final stage power amplifier (PA). A smaller percentage was also attributed to capacitor shorts on the RF output in the final stage.

Failure analysis revealed a majority of the pinch-off failures were related to shorted capacitors. In-depth analysis concluded failures were an interaction between the design of the circuit and a step in the process that charged up and destroyed the capacitors. Only capacitors where the bottom plate was connected to ground through a DFET source contact, were impacted. A proposed fix in the design was validated on an engineering lot where every other die was new design / old design, in a checker board layout on the reticle.

Employing optical microscope inspections by process engineering technicians and special Automated Optical Inspection (AOI) across several modules narrowed down the charging to two process steps; the top plate metal deposition and the subsequent field metal tape lift-off (TLO). Analysis of these inspections also concluded the new design eliminated the capacitor short, even on a wafer that suffered from an ESD event. Specifically, a wafer showed 78 sightings of blown capacitors from the old design, while zero from the new design.

INTRODUCTION

In semiconductor manufacturing, yield analysis and root cause investigations are necessary to improve yields and reliability. Yield improvement can have a positive impact on time-to-market, increased profit margins, on-time delivery to the customer, and improved performance and reliability. At a new product launch, it is critical to investigate failures, determine the root cause and implement a fix before ramping the product. This paper shows yield analysis driving yield improvement, sometimes leads to unexpected results. Fixing an issue seen on one lot, a product or a process flow, may also have a positive impact on the entire factory, improving overall yield and reliability. This involves taking the findings and rolling out a fab-wide project; a.k.a. best known methods (BKM).

FAILURE ANALYSIS

A low yielding wafer was pulled after laser dicing and ten failing die were chosen from the wafer for failure analysis. Initial optical inspection did not show any obvious anomalies. Since the low die sort yield was attributed to the pinch off related parameters in the final stage of the PA, this became the area of interest for manual probing and subsequent failure analysis (Figure 1).

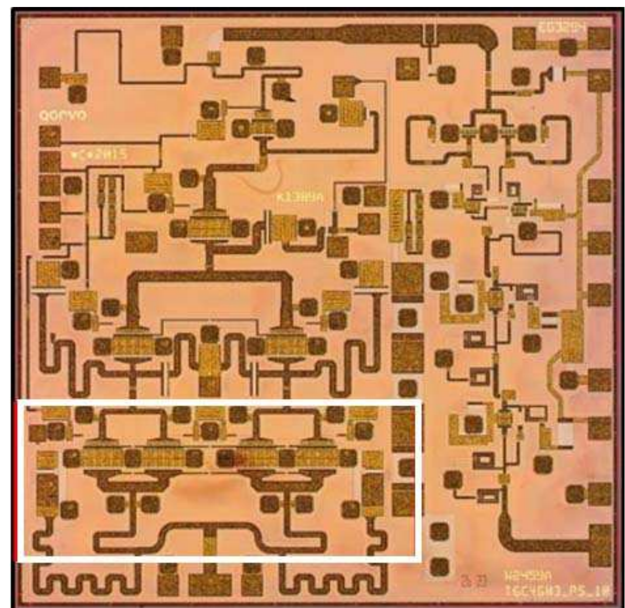

Figure 1: Optical image of a failing die. The area in the box shows the location of the final stage of the PA.

The die sort pinch off test was verified on the failure analysis bench by probing the 3rd stage drain with respect to the appropriate ground while supplying -2V on the gate of the 2nd stage PA pin. Note that on this wafer, the substrate vias are still not formed thus, the analyst was able to probe

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the two arms of the final stage independently. Nine out of ten die were not pinching off properly.

Liquid crystal analysis was performed on the nine dies that were not pinching off. On eight devices, a hotspot was generated on a capacitor that is connected in series with the 3rd stage drain pin and ground of the final stage (Figure 2).

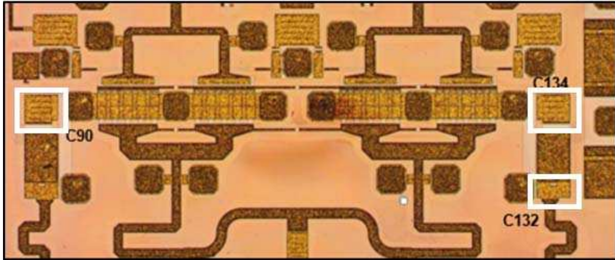

Figure 2: Partial optical image of a representative die showing the locations of the shorted capacitors (rectangles) obtained during liquid crystal analysis.

All devices with hotspots generated on a capacitor were chemically delayered using KII and H2O2 to remove the gold layer and the TiW layer respectively. Figure 3 shows the optical image of a die showing the ESD-like damage on the capacitor.

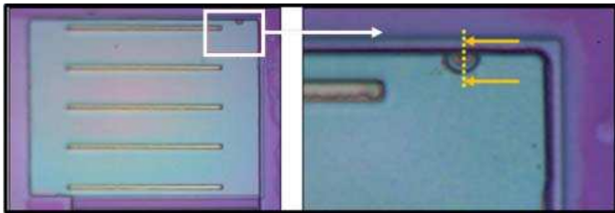
Figure 3: Optical images of the shorted capacitor C134 on a die showing the ESD-like damage (box). The dashed line shows the direction of FIB cross-section while the arrows show the direction of view.

FIB cross-section of the shorted capacitor confirmed ESD damage (Figure 4). In addition, it was also observed that the PSN layer covered the high current damage completely, suggesting that the ESD event occurred in between the capacitor top plate deposition and the subsequent PSN layer.

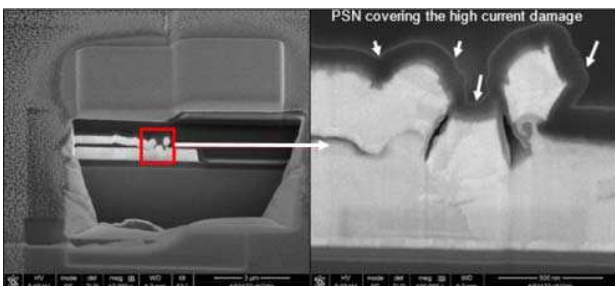

Figure 4: FIB cross-section of the ESD-like damage on capacitor C134 of a die (box). Note that the PSN layer is covering the high current damage completely suggesting that the ESD event occurred during the fabrication process, not at die sort or failure analysis.

Defect Influenced by Specific Design

A deeper dive into the failing units revealed the failures were always the same, specific capacitors, found only in the final stage of the PA. Die sort parametric data also confirmed the pinch off issues to be final stage related as well as a significant yield loss due to capacitor shorts of the RF output capacitor in the final stage. Not all capacitors in the circuit are capable of being tested at die sort, hence the capacitors that did not see a capacitor leakage test, showed up as pinch off failures. A review of the design revealed the bottom plate of these failing capacitors to be connected to the substrate through the source of a massive DFET. Capacitors that were floating (not attached to the source of a multi-finger DFET) did not have failures. This crucial finding would later help narrow down the cause by making the in-line visual inspections of capacitors limited to these specific locations. Moreover, the layout of the final stage could be changed by disconnecting the capacitor's bottom metal layer from the source and then evaluated for capacitor shorts.

Investigation for Defect Origin

As previously mentioned, the SEM image (Figure 4) shows the damage took place in-inline, prior to the PSN that covers the completed MIM capacitor. However, it was unclear if the damage occurred after the MIM PSN deposition or any other subsequent step in fabrication of the top plate of the capacitor. In order to determine the step at which capacitors are impacted by ESD, engineering material of this product would have to be started and inspected at multiple steps.

Using a high-velocity continuous process improvement (HV CPI) mentality, design engineering quickly redesigned the circuit and disconnected the bottom plate from the source of the FETs (Figure 5). Working very well as a team, Fab, Quality Assurance and Design engineering decided to order a set of engineering reticles that created a checker board of the original design and new design (disconnected metal), side by side across the reticle field; version A and version B, respectively. The benefit of the two design versions on the reticle allows the ESD event to cause damage to the version A design, indicating the operation responsible for the ESD, while inspection of the version B design at this step would validate the design fix.

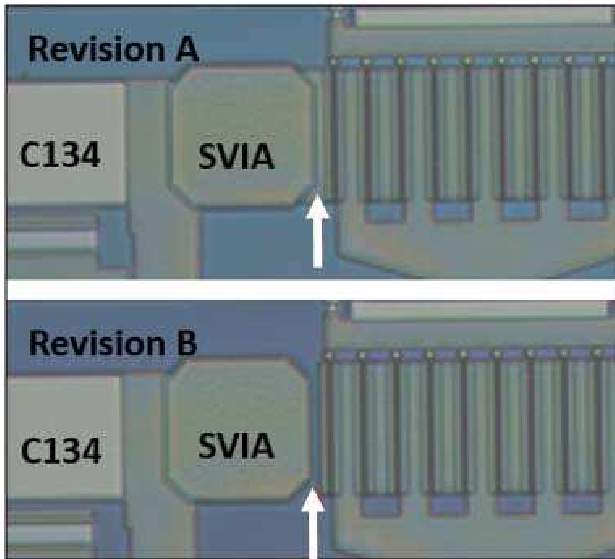

Figure 5: Optical images showing the bottom plate of the capacitor C134 is connected to the source of a DFET in version A, while the redesigned version B, the metal connection is removed. The capacitor is connected to ground through an SVIA.

Upon arrival of the new reticles, a number of wafers were started and moved swiftly to the first inspection step, post-MIM PSN deposition. This is the standard step for MIM AOI, however the AOI engineer created a special recipe that would only look at the specific capacitors in question. Moreover, the AOI recipe would only look at one of the versions at a time. This allowed data and images to be collected and analyzed separately, without any potential mix ups or laborious data filtering; another example of high velocity action. AOI indicated no ESD defects at this step.

Over the next few of days, fab engineering technicians performed manual optical inspections throughout various processing steps. The damage was finally found after the top plate lift off resist strip. Only five defects were found, all on the version A design. The special AOI recipe was run again at this step. The results indicated only one wafer with ESD damage. The wafer had 75 blown capacitors for version A, while zero for version B. All images were reviewed and many were heavily scrutinized in the tilt SEM (52 degree tilt) to learn more about the nature of the ESD and validate the new design is a fix.

SEM images of a blown capacitor found after lift-off resist strip revealed the event took place while field metal was still present on resist, fusing the field metal to the top plate of the capacitor (Figure 6).

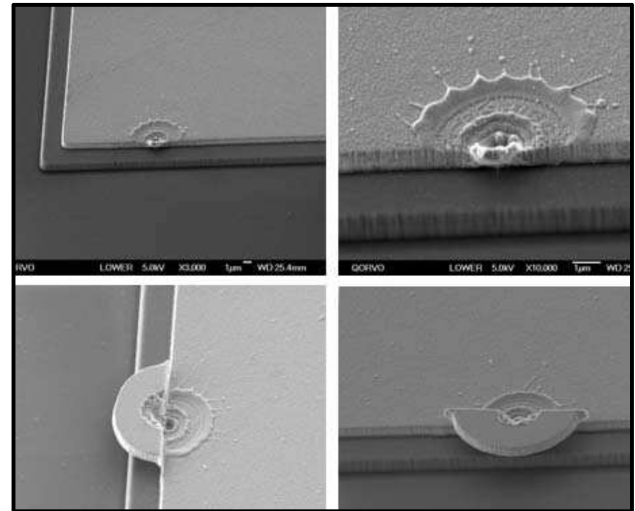

Figure 6: SEM images of the ESD damage on capacitors from a version A inspection. Note the remnants of the field metal layer are fused by arcing to the top plate of the capacitor.

The process steps involved to make the top plate are photo patterning, top plate metal evaporation, lift-off and cleans. Figure 7 helps illustrate what the device would look like just prior to the ESD event and where the arcing would occur. The photo pattern is defined, the metal deposited, and the structure is ready for metal lift-off.

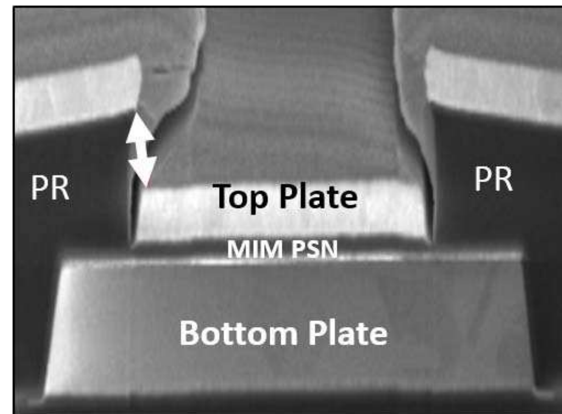

Figure 7: FIB cross section of the MIM capacitor prior to lift-off. The arrow indicates where the ESD event would create arcing between the top plate of the capacitor and the field metal prior to lift-off. PR is the photo resist.

The remnants of the field metal was a key piece of evidence that narrowed down the potential process steps where the wafer charged up and the ESD event occurred; the top plate metal evaporation and the subsequent tape lift-off (TLO).

DEFECT ELIMINATION

Investigation into the evaporator operation revealed the wafer wands used to manually unload the wafers from the dome after metal deposition were not grounded. The model to explain the damage at this step would be a charged wafer wand, making contact with the backside of the wafer, discharging through the wafer's substrate, the FET and across the capacitor to the field metal. In this case, it was found that the first wafer to be unloaded was the wafer with ESD damage.

The other process operation in question is the TLO. At this operation, a spool of adhesive tape is rolled over a wafer, pressed on firmly, and then peeled off, removing the field metal. The wafers are then cleaned up using solvent and are ready for inspection. The TLO tool has an ionizer that showers positive and negative ions to keep the charge buildup neutral. At this step, it is possible the ionizer is not working properly or is inadequate to prevent charge build up before or during the rolling process. Contact between the wafer and the electrostatically charged tape could result in discharge to field metal to the cap and down through the substrate. The tape TLO tool has been thoroughly investigated with a charge meter under static conditions as well as while running wafers. The in-tool ionizer shower is operating per manufacturer's specifications and wafers do not build up charge at this process operation. Finally, proper clean room ionizer functionality around these two tools has been verified and is operating as per specification.

The design change, successful in the elimination of capacitor failures related to ESD damage, is now the standard design used in production. This design methodology is now considered a best known method (BKM), such that it is the strongest means of protection against an ESD event in the MIM capacitor process formation.

CONCLUSION

A cross-functional team spurred failure analysis, a redesign of capacitor interconnect rules and automated optical inspection to find the root cause of die sort yield loss. The yield fallout was related to an ESD event during the MIM capacitor top plate fabrication. By grounding wafer wands at the metal evaporation operation, the ESD mechanism has been eliminated.

Two major benefits that this project highlighted were the importance of charge elimination during the fabrication process and robust design techniques to prevent die sort yield loss and potential reliability issues.

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ACRONYMS

pHEMT: pseudomorphic high-electron mobility transistor
DFET: Depletion-mode field effect transistor
ESD: Electrostatic Discharge
PA: Power Amplifier
TLO: Tape Lift Off
AOI: Automated Optical Inspection
DRC: Design Rule Check
MIM: Metal Insulator Metal (Capacitor)
PSN: Silicon Nitride
HV CPI: High Velocity Constant Process Improvement
SVIA: Substrate Via
FIB: Focused Ion Beam
SEM: Scanning Electron Microscope
BKM: Best Known Method
PR: Photo Resist