Using Six-Sigma Methodology to Reduce Metal-Insulator-Metal Capacitance Variance

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Abstract

Yield is considered one of the most critical factors affecting the profitability of a wafer fab. Significant cost-savings can be achieved by improving package yield. At Qorvo NC wafer fab, the variance of metal-insulator-metal (MIM) capacitance has shown significant impact on device performance and package yield of certain products. Reducing the variance of MIM capacitance will improve profitability of the fab.

This paper reviews how Qorvo NC wafer fab carried out a continuous improvement project to utilize Six Sigma methodologies to allocate the root causes of MIM capacitance variance, and to reduce it by 36.4%. This improvement resulted in cost-savings of $635,000 per year.

INTRODUCTION

Plasma enhanced chemical vapor deposition (PECVD) silicon nitride is commonly used as the dielectric layer for metal-insulator-metal (MIM) capacitor for RF integrated circuit design. Several high-volume products have been found to be sensitive to MIM capacitance density variance. For these particular products, either a higher or lower MIM capacitance density can result in lower package yield. Tightening MIM capacitance density variance will improve package yield, resulting in cost-savings.

This continuous improvement project was submitted to the management team as a Six-Sigma project. After approval, a cross-functional team including Process Engineering, Equipment Engineering and Test & Yield Engineering was formed. The DMAIC methodology (Define, Measure, Analyze, Improve and Control) was utilized as a guideline for the project. This systematic method included: cost feasibility assessment of the project, measurement systems validation, determination of root cause(s), implementation of improvements, and establishment of controls, in an efficient and thorough manner. By the end of the project, MIM capacitance density standard deviation was reduced by 36.4%. This exceeded the goal initially set by the team and resulted in cost-savings of $635,000 per year.

SIX SIGMA DMAIC IMPROVEMENT CYCLE [1]

DMAIC is a data-driven improvement cycle consisting 5 steps (Define, Measure, Analyze, Improve and Control) [2].

1) Define: To identify and validate the improvement opportunity.
2) Measure: To identify critical measurements, establish baseline and to develop a methodology to effectively collect data.
3) Analyze: To identify and validate the root cause of the problem, sources of variation and potential failure modes.
4) Improve: To identify, evaluate and select the right improvement solutions.
5) Control Phase: To assure achievement of the targeted results, to disseminate lesson learned and identify replication and standardization.

Define Phase:

In the define phase, Module Product Engineers provided Voice-of-Customer data to translate and quantify PECVD process improvements into dollars saved in terms of product yield improvements. Though many products have good yield within current capacitance density specification limits, as shown in figure 1, some products were able to achieve higher yield if the capacitance density distribution was shifted either up or down. To attain yield improvement on different products, it was necessary to tighten the capacitance density distribution and to center it on target.

Considering potential cost can be introduced by tool upgrade, labor work and material, cost-saving calculations were made to justify the feasibility of this project. The Six Sigma team worked with the product and yield team to calculate the cost-saving prediction based on package yield improvement from capacitance density variance reduction, which consisted of the cost saving for each percentage of module yield improvement multiplied by the predicted future volume of these selected parts.

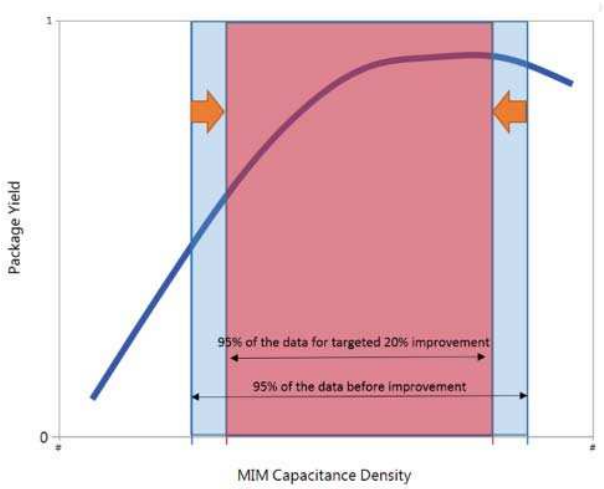

Figure 1. Example of a specific product: Yield vs. MIM capacitance density model curve

From this calculation, the team concluded that the goal for this project was to reduce the capacitance density standard deviation by 20%, which, in turn would achieve a module cost-saving of $400,000 per year.

Measure Phase:

In the measure phase, measurement systems were verified through Gage Repeatability and Reproducibility (GRR) studies, and data collected to set the baseline for the process.

First, GRR analysis was conducted on the reflectometry gages used for nitride thickness measurement and the ellipsometry gages used for refractive index measurements. Both tools showed good repeatability, providing the team with confidence that the data collected for these parameters was reliable.

Then, 6 months of capacitance density data was collected to set the process baseline. The capacitance density data was collected from electrical test results on process control monitoring (PCM) sites on the wafer. The capacitance density standard deviation was calculated and the process capability analysis was conducted. Two factors were observed to contribute to this variance: high within-tool variance on certain tools, and tool-to-tool differences.

On each CVD, three process parameters are collected daily as standard SPC: nitride thickness, nitride thickness non-uniformity and index of refraction (IR). As there are 5 wafers processed in a batch, the wafer-to-wafer non-uniformity is also characterized as the thickness variance within a batch.

An Ishikawa Fishbone Diagram was used to brainstorm, list and prioritize potential causes of high capacitance variance.

Analyze Phase:

In the analyze phase, the team compared capacitance density data for wafers processed on different CVD tools. Shown in Figure 2, this data was broken down to 3 parts: the mean value of capacitance density on each wafer (wafer mean), the moving range of wafer means, the range of capacitance density within each wafer (within-wafer range). This control chart method clearly shows the contribution of within-wafer differences, within-batch differences and tool-to-tool differences to the total capacitance density variance.

As shown in Figure 2, the wafer mean value was slightly different from tool to tool. More importantly, there was a significant difference of the capacitance density variance between the best tool and the worst tool. The top chart indicates the distribution of the wafer mean capacitance density on the worst tool (CVD6) is twice as wide as the best tool (CVD5). The middle chart shows that the moving range of wafer mean is much higher on CVD6. The bottom chart shows that within-wafer variation is also higher on CVD6. Nitride thickness was mapped on all five positions on the platen on all CVDs. The nitride thickness variance matched well with the capacitance density of wafers processed on the CVDs.

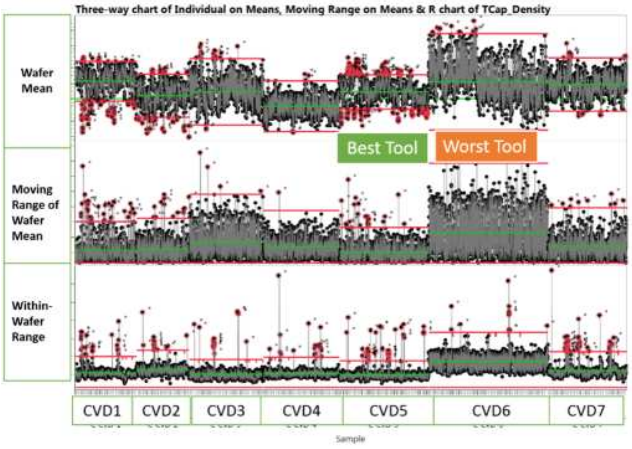

Figure 2. Capacitance density wafer mean, moving range, within-wafer range comparison for wafers processed on different CVDs.

To investigate the root cause of capacitance density variance, the team decided to compare the best tool (CVD5) to the worst tool (CVD6). Nitride thickness and IR data were compared. As shown in figure 3, the nitride thickness comparison variance is much higher on CVD6 than on CVD5.

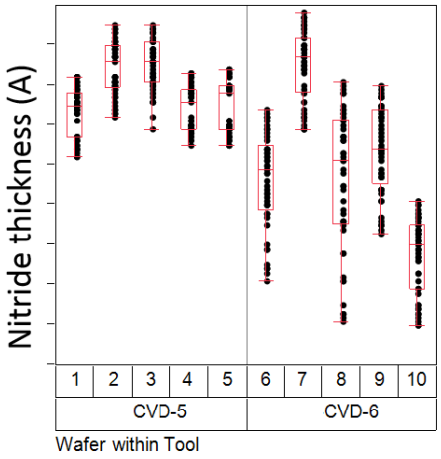

Figure 3. Nitride thickness difference for 5 wafers in a batch processed on CVD5 and CVD6.

This big tool-to-tool difference seemed more likely due to equipment differences between CVD tools. There were several factors listed on the equipment branch of Ishikawa Fishbone Diagram that were suspected contributors: platen temperature, wafer placement, showerhead cleaning, etc. The Equipment Engineer systematically compared the two CVDs. As shown on Figure 3, for CVD6 one position on the platen deposited thinner nitride than the other four. Wafer placement at this position was adjusted to ensure good contact between the wafer and the platen under vacuum. As shown in Figure 4, this approach improved the wafer-to-wafer difference, but did not improve the within wafer range for capacitor density. Another factor proven to affect nitride non-uniformity was the showerhead. Cleaning the showerhead temporarily improved nitride non-uniformity, but non-uniformity trended up with tool usage, as more by-product accumulated on the showerhead.

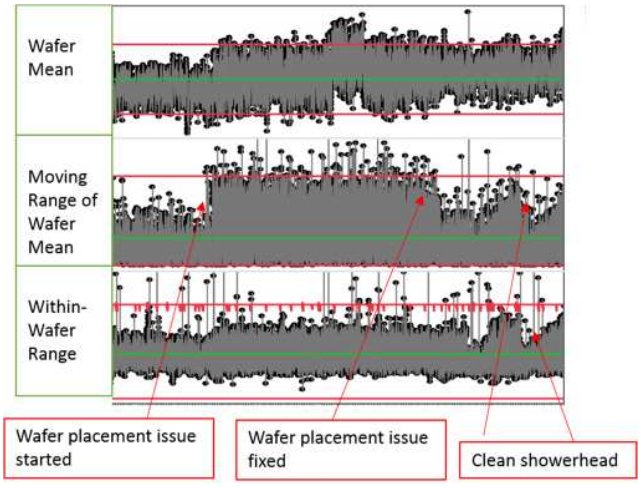

Figure 4. Nitride thickness trend with different tool activities on CVD6.

Other than wafer placement, showerhead impacts all 5 wafers processed in a batch. To understand the impact of showerhead, CVD5 and CVD6 showerheads were swapped. As shown in figure 5 and figure 6, after the showerhead swap, CVD5 gave uniform nitride deposition, while CVD6 gave non-uniform nitride deposition, similar to CVD5 prior to the change-over. The showerheads were switched back to their original tools and the non-uniformity trend followed with the showerhead. So showerhead proved to have the most significant impact on nitride thickness non-uniformity on the CVDs.

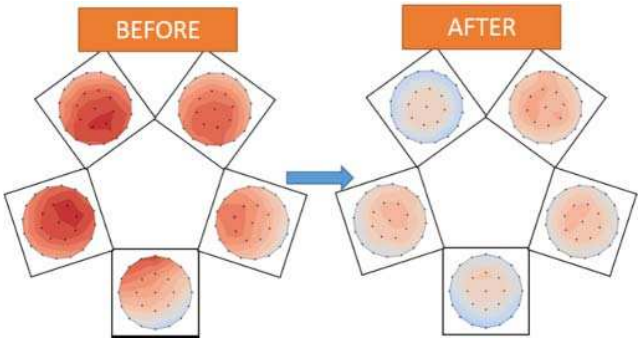

Figure 5. CVD6 (the worst tool) nitride deposition thickness before and after swapping showerhead with CVD5.

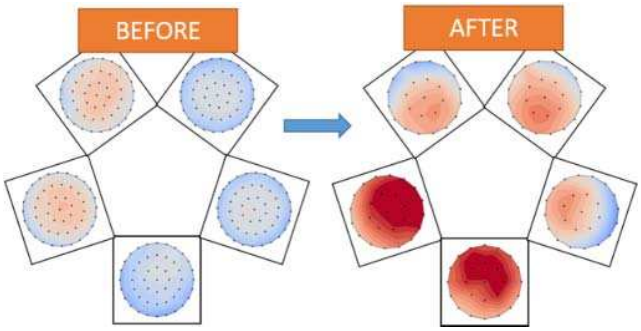

Figure 6. CVD5 (the best tool) nitride deposition thickness before and after swapping showerhead with CVD6.

A new showerhead was installed on one CVD. The nitride thickness standard deviation was reduced by 40%, which correlated to 22% improvement for capacitance density standard deviation.

In the Analyze phase, the team found the root cause for capacitance density variance was from nitride deposition thickness variance due to wafer placement and showerhead lifetime.

Improve Phase:

As showerhead lifetime was shown to have the biggest influence on nitride thickness variance, the decision was made

to change out showerheads on CVD tools. A small difference in dielectric constant of silicon nitride was observed on different CVDs, which resulted in a small capacitance density difference. Considering this difference and the costs associated with showerhead changes, the team decided to limit this nitride deposition process to three CVDs and change out the showerheads on all of them. When this proposal was submitted to management for approval, the cost of changing showerheads was easily justified based upon the cost-saving analysis performed in the define phase of this project.

As shown in figure 7, significant decrease of capacitance density standard deviation was observed as the project progresses. After these changes were implemented, new data was collected and analyzed. The initial goal of 20% standard deviation reduction was exceeded by 16.5%, translating into an annual yield improvement savings of $635,000.

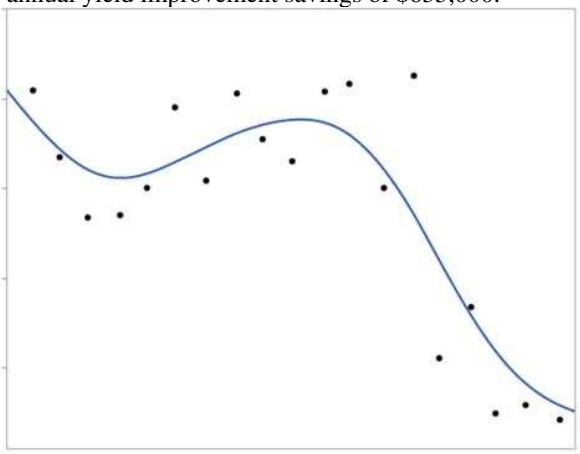

Figure 7. Monthly capacitance density standard deviation

Package yield was checked to confirm product improvements. As the example product in figure 8 shows, package yield has been improved significantly after different milestones of the project.

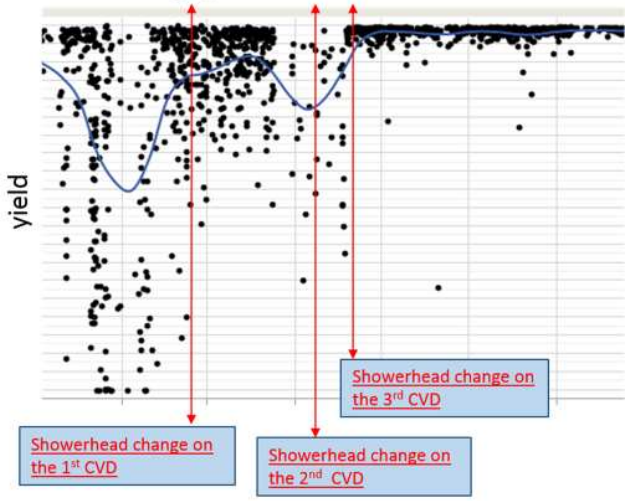

Figure 8. Yield improvement overtime for a certain product comparing with showerhead changes on designated CVDs.

Control Phase:

As the last step in the DMAIC cycle, control phase ensures that short-term improvements can be sustained for the long term. The following controls were implemented for long-term process monitoring:

1. Monitor the capacitance density. Team will take action when the capacitance density standard deviation increases above the threshold value. Three strategies are considered:
   1) Evaluate nitride thickness target.
   2) Change out showerhead on tools with high variance
   3) Target different nitride thickness on different CVD
2. Silicon Nitride thickness, non-uniformity and refractive index monitoring is critical, as any silicon nitride thickness trending or shifting will cause higher capacitance density variance. Western Electric Rule 1, 2 and 4 are used for Statistical Process Control (SPC).

CONCLUSIONS

Six sigma methodology was used to reduce MIM capacitance density variance for improved yields and cost-savings. A cross-functional team was formed to collect voice of the customer information, verify project feasibility, check measurement systems, identify root-causes, improve the process, and implement controls for long-term process monitoring. The MIM capacitance density standard deviation has been reduced by 36.5% which resulted in a significant cost savings for the company.

ACKNOWLEDGEMENTS

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ACRONYMS

DMAIC: Define, Measure, Analyze, Improve, Control
PECVD: Plasma Enhanced Chemical Vapor Deposition
MIM capacitor: Metal-Insulator-Metal capacitor
SPC: Statistical Process Control
PCM: Process Control Monitor