Beyond Silicon CMOS: Progress and Challenges

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Abstract

The increasing difficulties for further scaling of Silicon CMOS without compromising performance is bringing the quest for investigating alternative channel materials. This paper reviews the latest development progress in channel materials, process and integration and discusses the remaining challenges for implementing the III-V/Ge CMOS technology for 7nm and beyond.

INTRODUCTION

For five decades, silicon CMOS technology has been successfully driven by aggressive device scaling to increase performance and reduce transistor cost. However beyond 14nm technology node, the increasing difficulties for further scaling down of Silicon CMOS without compromising performance is bringing the quest for investigating alternative channel materials. Among these, III-V and Ge compound semiconductors are very attractive due to their outstanding electron and hole transport properties. This paper reviews the latest development progress in channel materials, process and integration and discusses the remaining challenges for implementing the III-V/Ge CMOS technology for 7nm and beyond.

CHANNEL MATERIAL ENGINEERING: MOBILITY ENHANCEMENT

Beyond traditional silicon as a channel material for MOSFET, the high mobility materials such as thin compressed silicon germanium (cSiGe) on silicon have been adopted for tuning threshold voltage of the P-type transistors (PMOS) using high-K/Metal-Gate dielectric and for boosting transistor performance for 28nm technology in high volume manufacturing [1]. The cSiGe channel engineering is also extensively developing for 22nm down to 10nm node with a different strain level and Ge content by using local Ge condensation. The local Ge condensation has first developed in early 2000, by a group of researchers in Japan [2] and today it is implemented in manufacturing [3,4]. While co-integrating of SiGe channels on Si for complete SoC application has been proven, several hurdles remain before the III-V and higher Ge content SiGe or Ge channels can be successfully implemented for further boosting performance and without compromising leakage, yield and cost.

In the past 5 years, the higher mobility and injection velocity materials such as germanium and III-V, their electronic properties are summarized in Table 1, are also extensively developed using either blank epitaxial film grown on silicon or on lattice matched substrate. Such substrates are used as donors, where the high quality high mobility film is bonded and transferred on insulator, forming GeOI, III-VOI substrate, Fig. 1 [5,6,7].

Table 1: Material properties of silicon and high mobility channel materials

Parameter	Si	Ge	GaAs	InP	$In_{0.53}Ga_{0.47}As$	$In_{0.7}Ga_{0.3}As$	InAs	InSb
Lattice constant (Å)	5.431	5.658	5.653	5.869	5.8687	5.937	6.058	6.4793
Band gap (eV)	1.12	0.66	1.42	1.34-1.35	0.74	0.58	0.35-0.36	0.17
Hole mobility (cm^2/Vs)	430-450	1900	400	150-200	300	400	460-500	850-1250
Electron mobility (cm^2/Vs)	1500-1600	3900	8500-9200	4600-5400	12000	20000	33000-40000	77000-80000
Effective density of states in valence band, N_V (cm^{-3})	1.04×10^{19}	6.0×10^{18}	7.0×10^{18}	1.1×10^{19}	5.5×10^{18}	5.9×10^{18}	6.6×10^{18}	7.3×10^{18}
Effective density of states in conduction band, N_C (cm^{-3})	2.8×10^{19}	1.04×10^{19}	4.7×10^{17}	5.7×10^{17}	2.1×10^{17}	1.6×10^{17}	8.7×10^{16}	4.2×10^{16}
Dielectric constant, k	11.9	16	13.1	12.4	13.9	NA	15.5	17.7
Melting point, T_m (°C)	1412	937	1240	1060	NA	NA	942	527

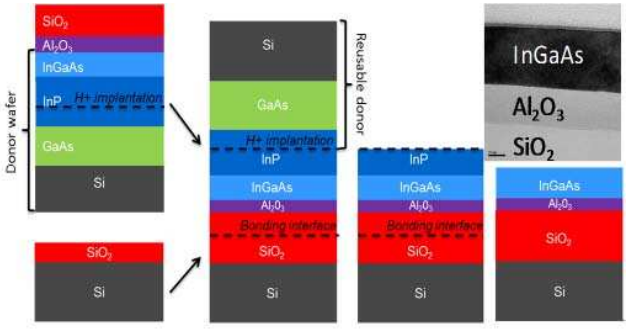

Figure 1: 300mm InGaAsOI wafer bonding with good crystallinity [7]

Another approach includes selective epitaxial growth on silicon using SiO_2 isolation structures, which allows defects to be confined and trapped at the bottom and at the vertical IIIV epi/oxide interface. This approach is known

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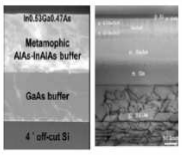
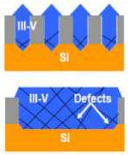
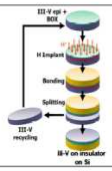
as "Aspect Ratio Trapping" (ART) [8]. Other more sophisticated approach includes, "Confined Epitaxial Lateral Overgrowth" (CELO) as summarized by Czornoma et.al. in Table 2 [9].

Table 2: L. Czornomaz, IBM Zurich, ECS 2014 [9]

Graded buffer	Defect Trapping	Wafer bonding
		
IEDM'10/11 (Intel, IQE, Sematech...)	IEDM'11, VLSI'14 (Sematech, IMEC)	IEDM'12/13 (IBM) VLSI'11 (UTokyo)
TDD low 10^8 cm^{-2}	TDD low 10^8 cm^{-2}	TDD <10^5 cm^{-2}
No co-integration	No "On-Insulator"	No large scale wafer

Despite all the efforts, the high defectivity and/or cost of the high mobility material growth are still far from reaching the level of maturity needed for adoption in the next 5 years.

DEVICE ENGINEERING: ELECTROSTATIC IMPROVEMENT

Since the insertion of Ge and III-V channel material are being considered for 7 or 5 nm technology node, an excellent gate or electrostatic control is required for scaling CMOS devices down to sub 15nm gate length. Thus innovation in device architecture such as fully depleted planar or multi-gate device architectures must be implemented for Ge and III-V channel devices. A lot of simulation predicted that an excellent electrostatic control down to 13nm gate length can be achieved for Ge or III-V multi-gate transistors, but experimental work can only demonstrate good electrostatic control behavior of Ge and III-V transistors with longer gate length (Lg>50nm). These multi-gate transistors or FinFET can achieve an acceptable short channel effect (SCE) with sub-threshold swing (SS) less than 120mV/dec and drain-induced barrier-lowering (DIBL) less than 120mV/V as shown in Figures 2 and 3, respectively [10].

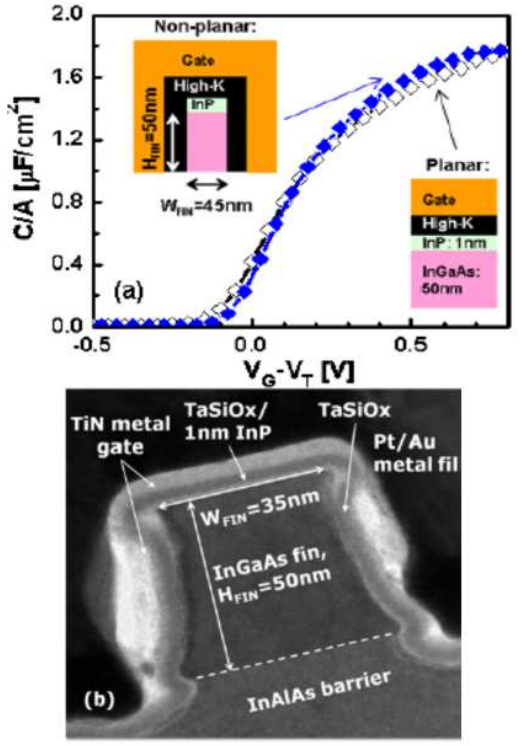


Figure 2: a) Capacitance-voltage characteristic planar vs. non-planar, multi-gate transistor or FinFET; b)TEM x- session of InGaAs FinFET [10]

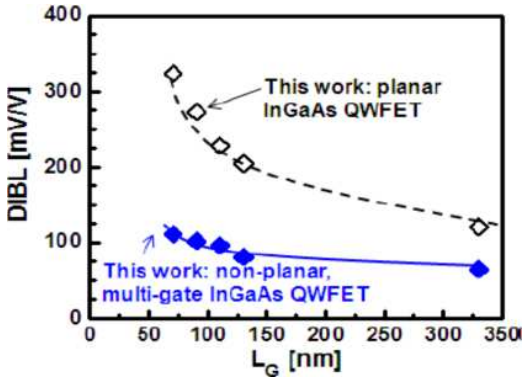


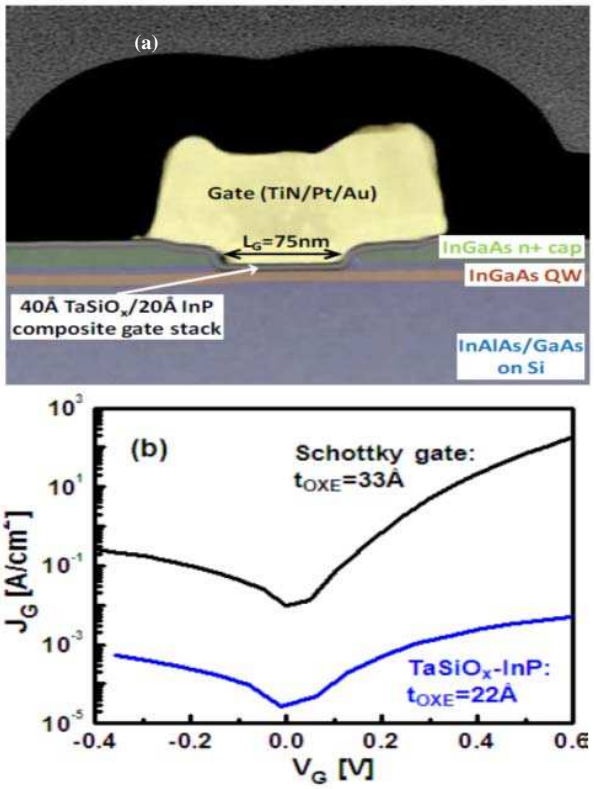
Figure 3: Drain-induced barrier drain vs. gate length (Lg) for planar and non-planar, multi-gate transistor or FinFET [10]

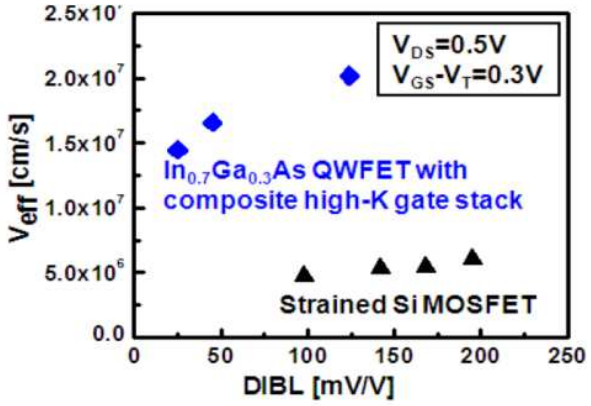
Ge/III-V/Si CO- INTEGRATION

The innovative high mobility material must be compatible with Si substrate to fully utilize the existing circuit platform. Thus it is necessary to co-integrate Ge and III-V materials with existing Si CMOS process flow and design rule of the insertion technology node. Tremendous efforts by researchers have been pursued in identifying for all channel materials a suitable high dielectric constant (K), metal gate stack and source/drain formation without degradation or compromising power/performance and a viable integration scheme. The objectives of the gate stack

is the equivalent oxide thickness (EOT) of 1nm or thinner, fixed charge trapping and interface charge trapping (Dit) less than 1E12/cm^2 to minimize mobility and reliability degradation. Most challenge is identifying the gate stack and source/drain formation that can satisfying Dit and parasitic resistance for Si, Ge and III-V transistors without significantly increasing complexity or compromising other devices or circuits.

Recent research demonstrated the integration of an advanced composite high-K gate stack (4nm $TaSiO_x$-2nm InP) in the $In_{0.7}Ga_{0.3}As$ quantum-well field effect transistor (QWFET) on silicon substrate, with thin EOT and low gate leakage and effective carrier confinement and high effective carrier velocity (V_{eff}) in the QW channel, Fig 4. (11).

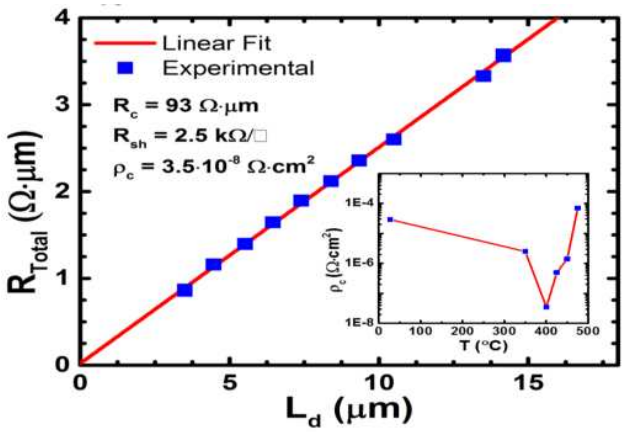




(c)

Figure 4: a) TEM cross-section $In_{0.7}Ga_{0.3}As$ QWFET with 2nm InP upper barrier layer & 4nm ALD-deposited TaSiOx high-K gate dielectric; b) Gate leakage (JG) vs. VG; c) Measured effective electron velocity vs. DIBL

Although InGaAs n-type FinFET shave attracted much interest for integration into future CMOS technology because of their extraordinary transport and scaling properties, progress in III-V p-channel transistors is lagging. Recent work showed that among majority of the III-V semiconductors, the antimonide system,$In_xGa_{1-x}Sb$ with $0<x<1$, is most promising due to its high hole mobility and its strong response to compressive stress [12,13]. Planar InGaSb HEMT [14] and MOSFET [15,16] prototype have been demonstrated with outstanding characteristics [17]. Si-compatible ohmic contacts with ultra-low contact resistivity of $3.5\cdot10^{-8}\Omega\cdot cm^2$ was also successfully realized, Fig. 5.



(a)

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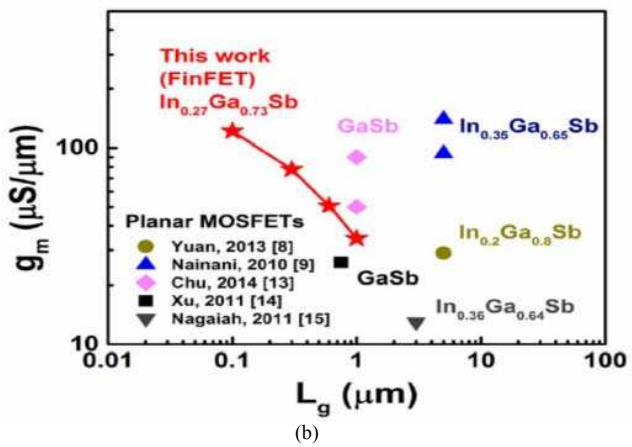
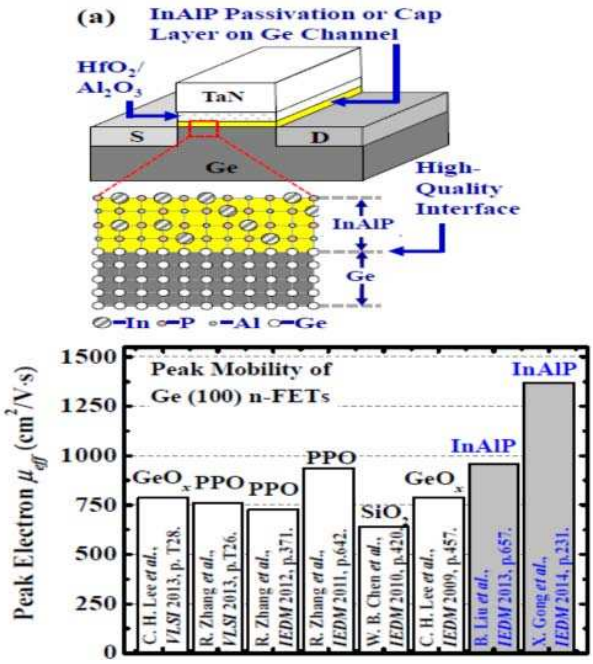
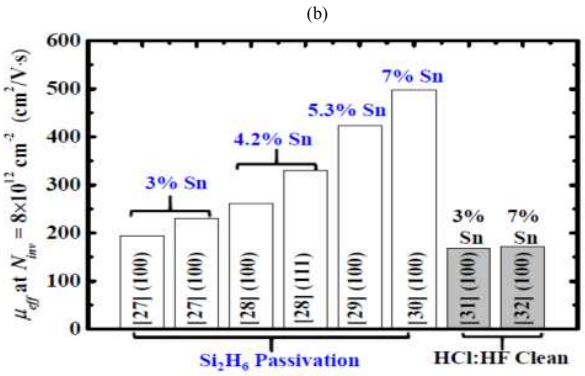


(b)

Figure 5: a) Si-compatible Ni/Ti/Pt/Al ohmic contacts top+-InAs measured by circular TLM; b) Maximum gm vs. Lg of recently published InGaSb MOSFETs.

Ge has the highest hole mobility among common elemental and compound semiconductors, and an electron mobility that is two times larger than that of Si. Ge is thus a promising channel material for future CMOS. Ge transistors need an advanced high-k metal gate stack, preferably formed using a common gate stack process. To achieve high carrier mobility, several interfacial layers such as GeO_2, YGeO, SiO_2/Si and InAlP were investigated. The TaN/HfO_2/Al_2O_3/InAlP(2.3 nm)/Ge stack, may be used for both n- and p-FETs, deliver high channel mobility, and leakage issues related to its small bandgap[18]. It was also demonstrated that incorporating Sn into Ge forms GeSn with an increased hole mobility for application in p-FETs, Fig. 6.[18].





(c)

Figure 6: a) Schematic showing a novel InAlP layer sandwiched between the Ge channel and high-*k* gate dielectrics for achieving high carrier mobility in Ge CMOS. InAlP is single crystalline and lattice matched to Ge, b) Record high peak electron *μeff* of 1370 cm^2/V·s was achieved for Ge (100) n-FETs using InAlP interfacial passivation; c) Comparison of *μeff* extracted at *Ninv* of 8×1012 cm-2 for GeSn p-FETs. Si2H6-passivated GeSn p-FETs exhibit much higher hole mobility

$Si_{1-x}Ge_x$ and $In_xGa_{1-x}As$ have been intensely researched as alternative channel materials for p-FETs and n-FETs, respectively, in CMOS logic applications [19-21]. Successful demonstrations of monolithic integration of Ge P-FETs and InAs N-FETs on Silicon Substrate with sub-120 nm III-V Buffer, sub-5 nm Ultra-thin Body(UTB),common raised S/D, and gate stack modules was demonstrated, Fig. 7, 8[21].

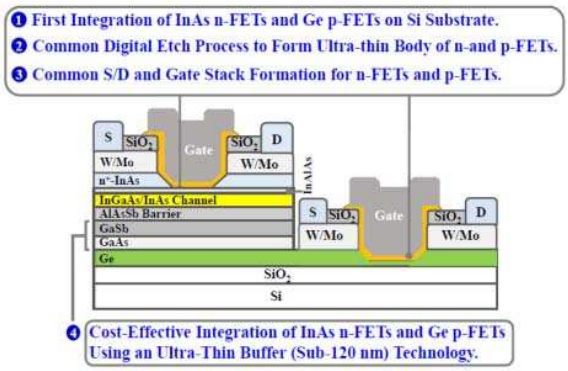


Figure 7: Key highlights: First demonstration of InAs n-FETs and Ge p-FETs monolithically integrated on Si substrate;

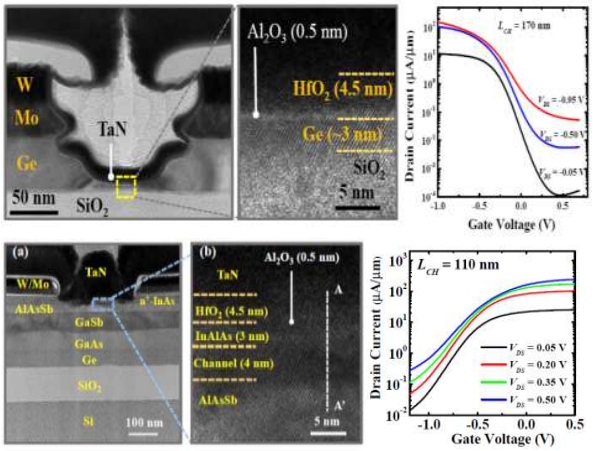


Figure 8; a) Ge p-FET on Si substrate with gate stack; b) InAs n-FET on Si substrate with gate stack

This 3D approach, as shown in Fig. 9, could be a viable solution to solve the complexity of co-integration and avoid performance/leakage compromising due to co-integration of all Si, SiGe/Ge and III-V devices into one plane. More importantly, transferring and stacking the high quality Ge or III-V thin film on insulator for fabricating the low-temperature UTB Ge or III-V devices over Si and SiGe CMOS could be a viable way to implementing the ultra-high mobility materials for high performance logic/RF and/or optical interconnect. This approach could reduce the impact of threading dislocation density in the S/D leakage and does not require the aggressive scaling of gate length for density due to the advantage of 3D which features more active area in a same layout area or form factor.

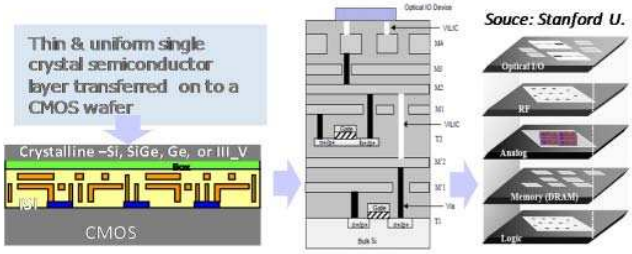


Figure 9: III-V n-FETs or Ge p-FETs monolithically integrated on Si CMOS substrate;

We discuss recent research progress in advancing Ge and III-V based transistor technologies. Approaches that address the key issues related to process, device, and integration of Ge and III-V based transistors are discussed. Although significant progress has been made, depending on what emerges as the best option for the p-channel device and the n-channel device, two or three dissimilar materials might need to be integrated side by side in very close proximity or on top of a Si wafer. Key challenges remain and industry is working on reaching cost effective integration, a manufacturable and scalable mature processes are needed for adoption in the next 5 years

CONCLUSIONS

Progress in researching alternative channel materials for p-FETs and n-FETs solutions for a Si based CMOS platform has been achieved. Such work paves the way for cost-effective and more mature integration for CMOS logic applications beyond Si.

REFERENCES

[1] H. R. Harris et al., VLSI Tech. Dig., p. 154, 2007
[2] T. Tezukaet. al., Jpn. J. Appl. Phys. 40, p. 2866, 2001
[3] Q. Liu et. al., IEDM, p. 9.1.1, 2014
[4] K. Cheng et. al., IEDM, p. 18.1.1, 2012
[5] E. Augendre et al., ECS Trans. 25 (7), p. 351, 2009
[6] W. Schwarzenbachet. al., Spring ECS, p., 2015
[7] J. Widiez et. al., SSDM, 2015
[8] N. Waldron et al., ECS Trans. 45 (4), p. 115, 2012
[9] LCzornoma et. al., ECS 2014
[10] M. Radosavljevicet. al., IEDM. P. 6.1.4, 2010
[11]M. Radosavljevicet. al., IEDM. P. 319, 2009
[12] J. A. del Alamo, Nature, v. 479, p. 317, 2011
[13] L. Xia et al., Appl. Phys. Lett., v. 98, p. 053505, 2011
[14] L. W. Guo et al., IEEE Electron Dev. Lett., v. 36, p. 546, 2015
[15] Z. Yuan et al., IEEE Electron Dev. Lett., v. 34, p. 1367, 2013
[16] A. Nainani et al., IEDM Tech. Dig., , p. 6.4.1, 2010
[17] Wenjie Lu et. al., IEDM, p. 819, 2015
[18] Yee-Chia Yeoet. al.,IEDM, p. 28, 2015
[19] C. Huang et al., IEDM, p. 586.2014
[20] K. Tomiokaet al., IEDM, p. 89.2013
[21] H. Schmidet al., APL 106, 23310, 2015
[22] S. Yadav et. al.,IEDM, p. 24, 2