Epitaxial Lift-off and Transfer of III-N Materials and Devices from SiC

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Keywords: Nb_2N, GaN, HEMT, LED, substrate reclaim.

Abstract

In this study, we present an experimental demonstration of a novel approach to epitaxial lift-off (ELO) and transfer of high quality III-N (GaN, AlN, etc.) materials and fully front-side-processed devices from SiC substrates. By using a single crystal Nb_2N sacrificial layer that is lattice matched to the underlying SiC substrate, III-N heterostructures of quality equivalent to those produced directly on SiC can be grown, processed into devices, and then released in a selective XeF_2 vapor phase etch. Measured electron transport data of released GaN HEMT test structures transferred to Si substrates shows that there is no substantial change in low-power density electrical performance introduced by the transfer process. In contrast to the well-known Smart Cut technique, material and devices released using the NRL ELO technique [1] have atomically smooth backsides (< 0.5 nm rms) that do not require further polishing prior to bonding to an alternative substrate.

INTRODUCTION

To extend wireless connectivity to an increasing number of devices surrounding us in everyday life, there is a growing need for small form factor, high performance mixed-signal integrated circuits. Heterogeneous integration, or the physical combination of circuits or circuit elements from various solid state technologies such as Si and compound semiconductors, is an emerging, cost-effective approach to address this need. By utilizing an integrated technology platform, the strengths and advantages of each material system can be combined into a single chip.

SiC, GaN, and related III-N materials have clearly demonstrated an advantage in RF power amplification, solid state LEDs/lighting, and power switching applications in the recent past. However, their ability to be easily transferred from their original substrate and incorporated into a heterogeneously-integrated platform has been partially hindered by the chemical inertness of their substrate. Selective wet etching of SiC, GaN, and AlN is very difficult, and not practical in most instances, yet these substrates are desirable because they provide the best lattice match for low dislocation density heteroepitaxial material, which is required to achieve high electrical performance and device reliability.

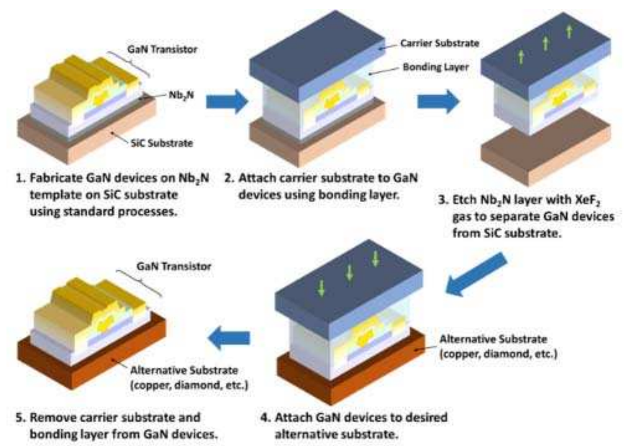

Figure 1. Epitaxial liftoff and transfer of GaN transistor from Nb_2N/SiC.

In this paper, we discuss a novel epitaxial lift-off (ELO) technique, illustrated in Fig. 1, that allows for III-N materials and devices to be removed from closely lattice matched substrates. To achieve separation and release of the epitaxial layers from the substrate, we use a thin layer of Nb_2N that can be sacrificially etched away in reactive XeF_2 gas.

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EXPERIMENTAL RESULTS AND DISCUSSION

The transition metal nitride Nb_2N is a hexagonal, metallic crystal that has a very low (0.7%) in-plane lattice mismatch with SiC. At NRL we have recently demonstrated the first thin film growth of Nb_2N on SiC using plasma-assisted MBE [2-3]. To investigate the utility of this novel material, we have used MBE to grow a N-polar GaN HEMT heterostructure on a 30 nm thick template of Nb_2N grown on a three-inch 6H-SiC wafer. The HEMT layer structure from bottom to top included a 100 nm AlN nucleation layer, 1.3 µm GaN buffer layer, 30 nm $Al_{0.4}Ga_{0.6}N$ barrier, and a 30 nm GaN channel layer. The TEM image in Fig. 2 shows that the N-polar GaN HEMT heterostructure grown on a Nb_2N/SiC template exhibits similar crystal quality to other HEMT structures grown directly on SiC.

After material growth, HEMT devices were fabricating using an ohmic-first process flow. Source and drain contacts were patterned using contact lithography and e-beam evaporation of a Ti/Al/Ni/Au (20/100/10/50 nm) metal stack. Prior to metallization, a low-power O_2 plasma was used to

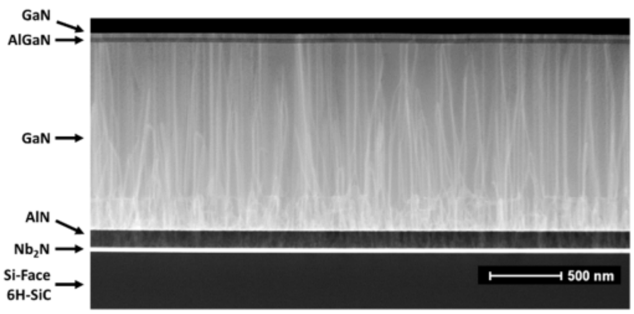

Figure 2. Cross-sectional transmission electron micrograph of a N-polar GaN HEMT heterostructure grown by MBE on an Nb_2N/SiC template.

clean the semiconductor surface, followed by a 30 s BOE dip, and deionized H_2O rinse. A 30 s rapid thermal anneal at 850 °C resulted in an ohmic contact resistance of 0.4 Ω·mm. Next mesa isolation was performed using a $BCl_3/Cl_2/Ar$ based dry etch. To reduce gate leakage current, a 10 nm thick ALD TiO_2 gate insulator was deposited at 300 °C, followed by e-beam evaporated Pt/Au (20/300 nm) gates that were patterned using contact lithography. Finally, contact vias were etched through the ALD TiO_2 gate insulator using a fluorine-based plasma, followed by a Ti/Pt/Au (25/25/400 nm) overlay metallization. The final device structure (without probe pads) is shown in Fig. 3, along with a photograph of the processed wafer. The drain current characteristics of a N-polar GaN HEMT with L_G = 1 µm, W_G = 2 × 75 µm, L_{GD} = 2.5 µm, and L_{GS} = 1.5 µm are shown in Fig. 4, and were found to be comparable to similar N-polar GaN HEMTs grown directly on SiC [4-5]. The device exhibited a maximum current density in excess of 1 A/mm and breakdown voltage of over 90 V (which was limited by vertical breakdown between the drain contact and Nb_2N layer.)

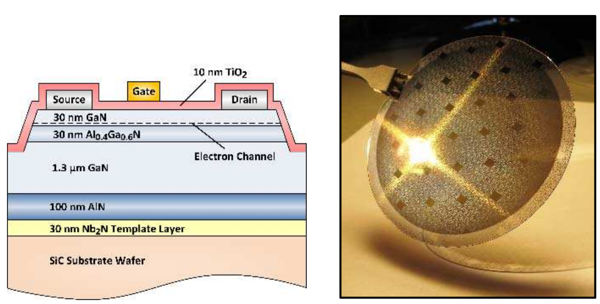

Figure 3. Layer structure of N-polar GaN HEMT on Nb_2N/SiC (left) and photograph of front-side processed 3” wafer implementation (right).

After device fabrication and electrical testing, a Ni hard mask was patterned using the mesa level photomask, followed by a deep mesa etch through the III-N and Nb_2N epitaxial layers using a $BCl_3/Cl_2/Ar$ ICP plasma. Selective removal of the hard mask was then performed in dilute nitric acid. The ELO release was achieved by laterally etching away the Nb_2N sacrificial layer using a XeF_2 etch at 100 °C.

Individual released GaN devices were transferred to Si by using a needle probe pressed into and affixed to Au-topped probe pads, as shown in Fig. 5a. Once the devices were attached to the probe, the substrate was dropped away, transferred out, and replaced with a bare Si wafer. Using a

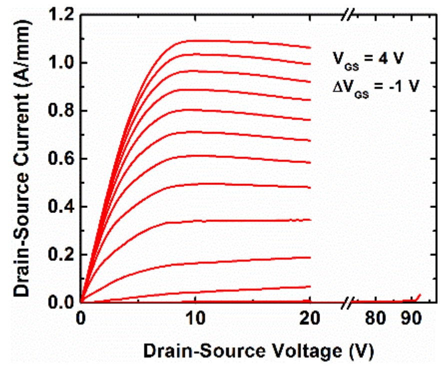

Figure 4. Drain current characteristics of a 1 µm gate length, 2 × 75 µm gate width N-polar GaN HEMT on Nb_2N/SiC before release.

second needle probe, the GaN structures could be placed on the Si wafer and evaluated using standard on-wafer electrical characterization (Fig. 5b). No bonding layer or adhesive was used between the GaN device and Si substrate in this study.

Table I shows results from on-wafer Hall effect measurements of van der Pauw structures before and after release/transfer to Si. The electron transport performance is nominally unchanged, suggesting that the mechanical integrity of the III-N material is still intact after transfer and the release processing does not cause damage to the devices.

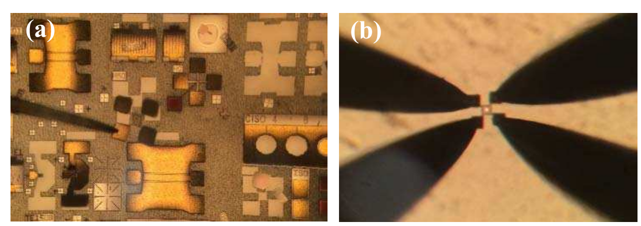

Figure 5. Van der Pauw test structure (a) after release and (b) transfer to Si.

TABLE I
ELECTRON TRANSPORT HALL EFFECT DATA

	R_{SH} (Ω/sq)	N_{SH} (cm^{-2})	Mobility (cm^2/V·s)
Before release	359	1.24×10^{13}	1408
After transfer to Si	353	1.30×10^{13}	1365

Long-gate HEMT devices with L_G = 50 µm, W_G = 60 µm, L_{GD} = 3 µm, and L_{GS} = 3 µm were transferred to Si using the needle probe transfer technique mentioned above. Fig. 6 shows micrographs of the device before and after transfer.

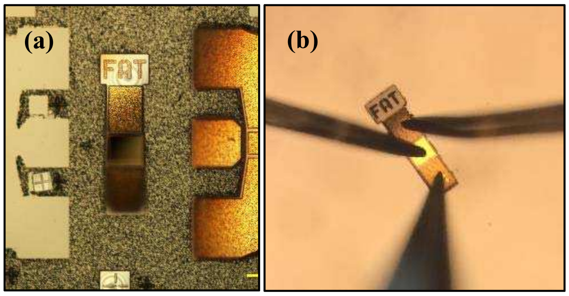

Figure 6. FAT FET test structure (a) after release and (b) transfer to Si.

The dc electrical performance was measured using needle probes and two source-measurement units. Fig. 7 shows the drain current characteristics of the long-gate HEMT before and after transfer to Si. In general, neither the on-resistance or modulation behavior of the device appears to change significantly after transfer. While the device had a relatively low drain current density due to the large source-drain spacing (L_{SD} = 56 μm), the negative slope of upper curves in the saturation region of Fig. 7 suggest that there may be increased self-heating in the transferred device. This is certainly plausible since the transferred device was only being held in contact with the Si substrate by force exerted by the needle probes. It is likely that by using thermal paste or epoxy, to bond the device to a high thermal conductivity substrate, the self-heating effect would be reduced or eliminated.

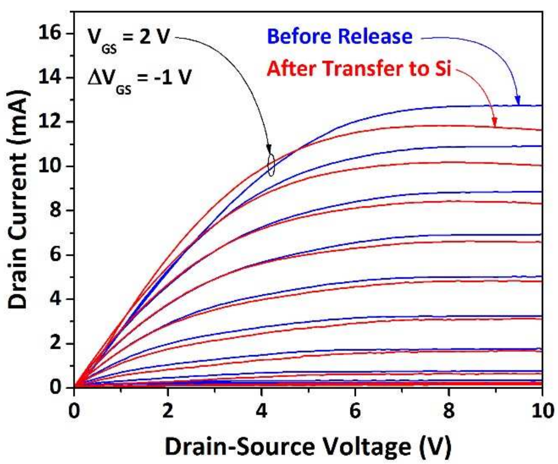

Figure 7. FAT FET drain current characteristics before and after release and transfer to Si.

Fig. 8 shows the transfer curve characteristics of the long-gate device before and after transfer to Si. The drain current levels are very similar, with only a slight reduction in maximum current and minimal shift in threshold voltage.

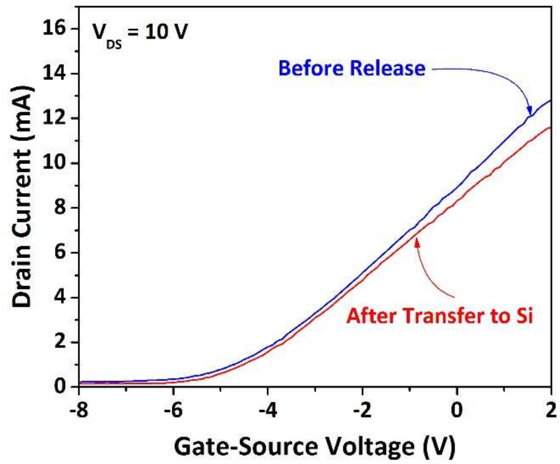

Figure 8. FAT FET transfer characteristics before and after release and transfer to Si.

While the long-gate HEMT results show that there is potential in the ELO release and transfer process, our ultimate goal in this study is to demonstrate transfer of an RF N-polar GaN HEMT in GSG configuration, such as the one measured in Fig. 4. Presently, due to a masking limitation on our mesa level design, we were unable to transfer the gate probe pad and connection tab needed to contact the 1 μm gates. However, we were able to measure the open channel (ungated) drain current characteristics of a transferred device with 75 μm width and L_{SD} = 5 μm and the results are shown below in Fig. 9. The data shows that the on-resistance of the FET channel does not change significantly after transfer. However, there is an appreciable drop in maximum current density, likely due to the poor thermal interface formed without a bonding layer.

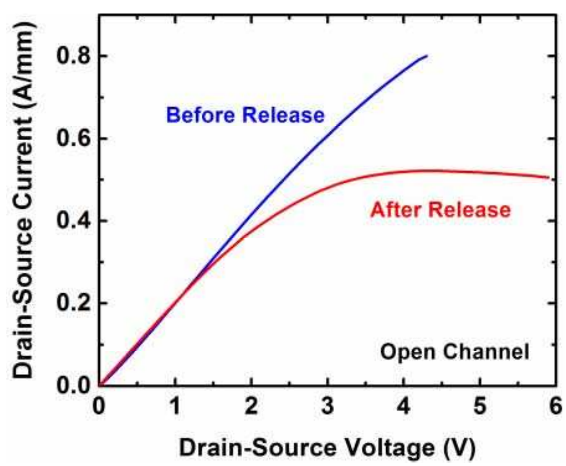

Figure 9. Open channel (ungated) drain current characteristics of a 75 μm wide, L_{SD} = 5 μm N-polar GaN HEMT before and after release.

To investigate the material properties of the backside of released GaN devices, AFM and XPS were used. AFM measurements, shown in Figs. 10 and 11, revealed that the backside of released GaN HEMTs were very smooth with rms roughness less than 0.5 nm. Present in some of the images, such as the one in Fig. 10, are lines that show that the AlN nucleation layer (and by inference the Nb_2N template layer) was grown conformally on the atomic steps

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of the SiC substrate. Fig. 12 shows a plot of AFM rms roughness versus scan size. The flat slope of the curve suggests that there are no large particles present that may inhibit planar bonding.

XPS measurements of the backside of a released device showed the presence of surface Nb (1 at. %) and F (11 at. %), in addition to Al, C, O, and N. However, after 45 s of Ar sputtering (which removed 1-2 nm of material), the measured Nb, F, and C signals dropped below XPS detection limits. This suggests that any residual Nb_2N and physisorbed or chemisorbed species that are introduced by the release process can be removed with simple cleaning procedures prior to device bonding to an alternative substrate.

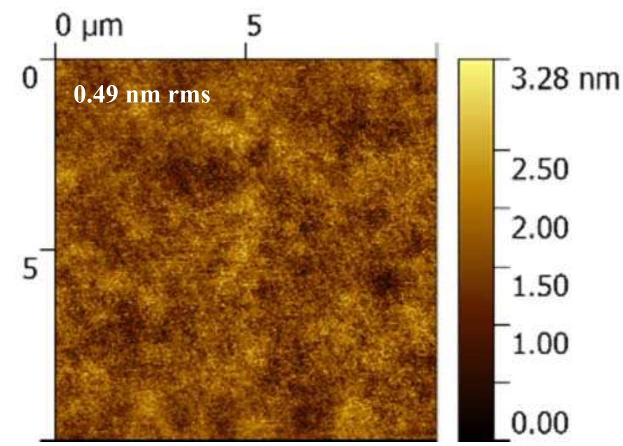

Figure 10. 10 × 10 µm AFM scan of the backside of a released GaN HEMT.

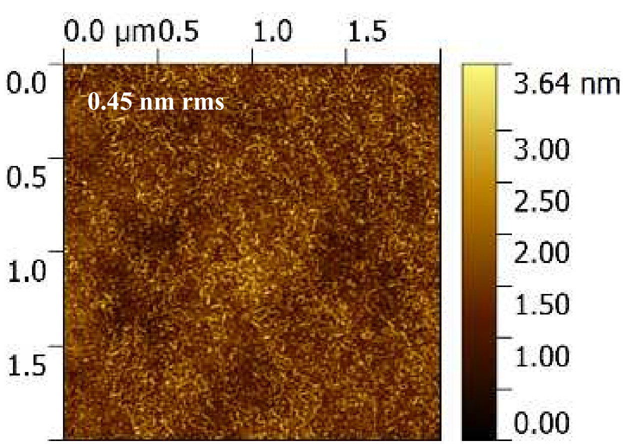

Figure 11. 2 × 2 µm AFM scan of the backside of a released GaN HEMT.

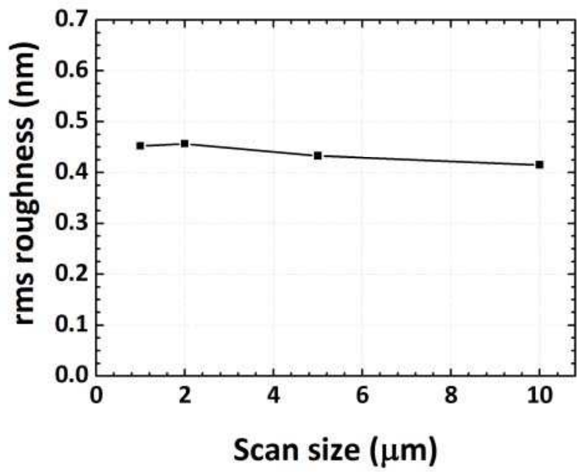

Figure 12. Average rms roughness versus scan size for several AFM scans of the backside of a released N-polar GaN HEMT.

CONCLUSIONS

The NRL ELO approach has several advantages over competing techniques for III-N device release and transfer. Since Nb_2N is thermodynamically stable with III-N materials, it has a large thermal budget for epitaxial overgrowth and/or high temperature device processing (i.e. ohmic RTA alloying). The interfaces in contact with the Nb_2N are atomically smooth after release, enabling direct bonding of GaN devices to alternative substrates and easy reuse/reclaim of GaN, AlN, or SiC substrates. Additionally, there is also potential for the growth and transfer of SiC materials and devices using this technique.

ACKNOWLEDGEMENTS

This work was supported by the Defense Advanced Research Projects Agency (D. Green) and by the Office of Naval Research. We gratefully acknowledge helpful discussions with K. Hobart and thank N. Green for assistance with device processing. The views, opinions and/or findings expressed are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

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ACRONYMS

AFM: Atomic Force Microscopy
ALD: Atomic Layer Deposition
BOE: Buffered Oxide Etch
ELO: Epitaxial Lift-Off
GSG: Ground-Signal-Ground
HEMT: High Electron Mobility Transistor
ICP: Inductively Coupled Plasma
MBE: Molecular Beam Epitaxy
RTA: Rapid Thermal Anneal
TEM: Transmission Electron Microscopy
XPS: X-ray Photoelectron Spectroscopy