GaN-on-Diamond: Robust Mechanical and Thermal Properties

Huarui Sun,[1] Dong Liu,[1] James W. Pomeroy,[1] Daniel Francis,[2] Firooz Faili,[2] Daniel J. Twitchen,[2] and Martin Kuball[1]

[1]Center for Device Thermography and Reliability (CDTR), H. H. Wills Physics Laboratory,
University of Bristol, Tyndall Avenue, Bristol BS8 1TL, United Kingdom
e-mail: martin.kuball@bristol.ac.uk Phone: +44 117 928 8734
[2]Element Six Technologies U.S. Corporation, Santa Clara, CA 95054, USA

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Abstract

Achieving robust mechanical and thermal properties in GaN-on-diamond is critically important for reliable next-generation high-power electronics based on this material system. The work described here demonstrates that excellent stress management and interfacial strength has been achieved, as well as homogeneous interfacial thermal properties across the wafer for the latest GaN-on-diamond technology.

INTRODUCTION

Over the past decade significant effort and progress has been made to integrate diamond with GaN-based electronics for improved thermal management. To date, GaN-on-diamond HEMTs have been demonstrated with outstanding performance for high-power microwave device applications [1,2]. Of the various GaN-diamond integration technologies, the Element-Six approach considered in this work involves removing the substrate from a standard GaN-on-Si wafer, followed by the deposition of a thin dielectric layer and the subsequent growth of CVD diamond on the exposed GaN surface. Stress management in the GaN and the mechanical stability of the GaN-diamond interface, owing to the large thermal expansion mismatch between these materials, is naturally a concern which arises. Moreover, the wafer-level homogeneity of mechanical and thermal properties is yet to be assessed.

In this paper, we use Raman spectroscopy to characterize the GaN layer stress in the manufactured GaN-on-diamond wafers, showing that this stress has nearly been eliminated through successive generations of wafer development. Using a micro-pillar based fracture test, we illustrate that the GaN-diamond interface has excellent mechanical stability. We further demonstrate a nearly homogeneous distribution of the effective thermal boundary resistance (TBR$_{eff}$) between GaN and diamond across a three-inch wafer using transient thermoreflectance mapping.

MEASUREMENT TECHNIQUE

Raman spectroscopy measurements were performed using a Renishaw InVia system with a 488 nm Argon laser. The E$_2$ peak with stress coefficient -2.7 cm^{-1}/GPa [3] was used to determine the inbuilt stress in the GaN layer, referenced to a stress-free value of 567 cm^{-1} measured for bulk GaN (consistent with previously reported values).

To assess the GaN-diamond interfacial strength, micro-pillars comprising the GaN/dielectric/diamond layer structure were created using focused Ga$^+$ beam milling. A force measurement silicon probe mounted on a micro-manipulator was used to apply controlled displacement or load to the GaN layer from the side of the micro-pillar. The force was measured by a piezoelectric sensor with a resolution of 0.1 μN. The deformation and the fracture process were monitored *in situ* in a scanning electron microscope (SEM).

The TBR$_{eff}$ at the GaN-diamond interface is a lumped thermal resistance with contributions from the amorphous dielectric layer with its lower thermal conductivity and the diamond nucleation layer formed in the initial phases of the diamond growth. To measure the TBR$_{eff}$, a contactless laser-based transient thermoreflectance technique was employed. A 355 nm pulsed laser is used to heat the GaN surface, inducing a rapid temperature increase, which subsequently relaxes due to heat diffusion into the layers. A 532 nm CW laser is used to monitor the surface reflectance change caused by the temperature rise as a function of time. The TBR$_{eff}$ between GaN and diamond is then extracted by
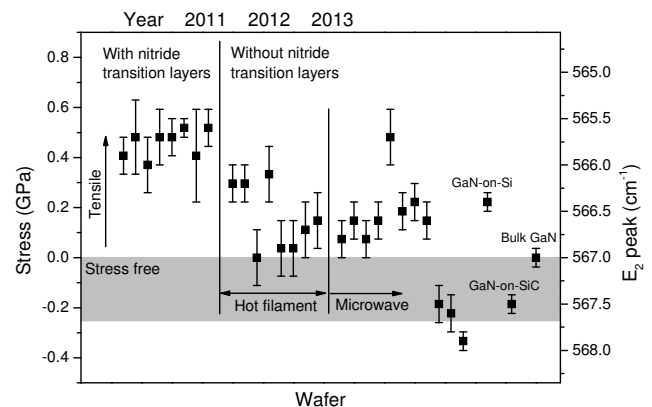
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Figure 1. The stress in the GaN layer determined by the Raman E$_2$ peak for various GaN-on-diamond wafers through successive generations of development. The grey area indicates E$_2$ peak positions in stress-free GaN from literature.

fitting the thermoreflectance transient with a finite element thermal simulation. The laser measurement system is integrated into an optical microscope with a motorized scanning stage; this enables rapid, high spatial resolution wafer mapping. More details of the measurement can be found in Refs. 4 and 5.

RESULTS AND DISCUSSION

The stress in the GaN layer was characterized for a number of GaN-on-diamond wafers from different generations spanning the development stages of this technology [6]. The result is displayed in Figure 1. In literature the stress-free E_2 peak is found to vary between 567 cm^{-1} and 567.7 cm^{-1} (grey area in Figure 1). For comparison, GaN-on-Si and GaN-on-SiC wafers were also measured and included in the plot. Prior to year 2011, the micron-thick nitride transition layer originally from the GaN-on-Si wafer was kept between the GaN and diamond. These early wafers show a tensile stress of 0.4 - 0.5 GPa. Later wafers incorporated the removal of the nitride transition layer to lower the thermal resistance. Two diamond growth methods were then used: Hot filament (HF) CVD and microwave (MW) plasma CVD, of which the latter has become the industrial standard. From 2013 onward, the effort has been focused on optimizing the dielectric layer thickness and the diamond seeding method. The stress was alleviated and generally maintained at levels within ± 0.2 GPa for both HF (after 2012) and MW growths. This highlights the role of improving the interface in stress

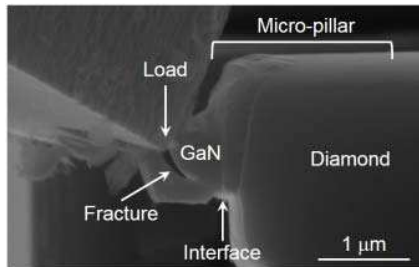Figure 2. *In situ* SEM graph of the micro-mechanical strength test. Fracture occurred in the GaN layer at a load of ~ 300 μN.

management, which is essential for achieving crack-free, large-size GaN-on-diamond wafers with low wafer bow.

The wafer for the micro-mechanical test consisted of a ~ 0.7 μm-thick GaN, a 40 nm-thick dielectric interlayer, and a 100 μm-thick MW diamond substrate. As illustrated in Figure 2, the whole structure was milled by focused Ga$^+$ ion beam to form a micro-pillar with the top GaN layer reduced to a smaller cross-sectional size than the diamond base for better loading control. Fracture occurred in the GaN layer when a load of 300 μN was reached, whereas the interface and the diamond remained undamaged. This translates to a principal stress at the GaN-diamond interface as high as 3 GPa, suggesting that the interfacial strength is greater than this value. The GaN-diamond interface is therefore considered to be stable from a mechanical point of view.

Figure 3 shows the TBR$_{eff}$ map of a three-inch GaN-on-diamond (MW) wafer with a 37 nm-thick dielectric layer. The measurement uncertainty is approximately ±10% considering the uncertainties in the GaN layer thickness and the specific heat of GaN used in the finite element simulation. The TBR$_{eff}$ is reasonably homogeneous across the wafer, with a slight increase from the center towards the edge. This confirms the uniform interface quality as well as consistently robust material bonding between GaN and diamond on a wafer level. These values are broadly comparable with GaN-on-Si and GaN-on-SiC wafers, and can be further reduced by optimizing the dielectric thickness and the diamond seeding [7]. The measurement technique could also be used for wafer inspection prior to HEMT fabrication. Any anomalies at the GaN-diamond interface
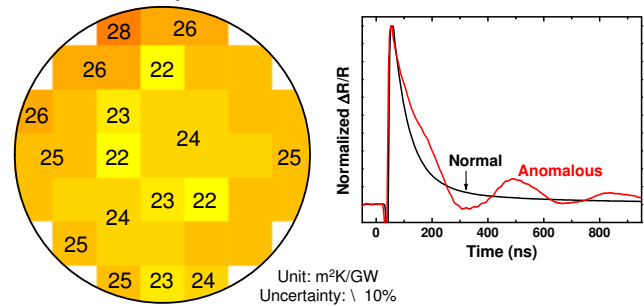

Figure 3. Three-inch GaN-on-MW diamond wafer and its TBR$_{eff}$ map. Representative thermoreflectance transients are shown corresponding to normal regions and a local imperfection (data from a different wafer, for illustration only), respectively.

would be apparent in the measured thermorefectance transient, as illustrated in Figure 3, enabling pre-screening of wafers.

CONCLUSIONS

GaN-on-diamond technology for high-power transistors has seen substantial progress in recent years. The stress in the GaN layer has nearly been eliminated through optimization of the diamond seeding and growth. The GaN-diamond interface exhibits great mechanical strength, and the interfacial thermal resistance is nearly homogeneous across the wafer. The robust mechanical and thermal properties lay a crucial basis for a reliable electronic device technology.

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ACRONYMS

HEMT: High Electron Mobility Transistor
TBR_{eff}: Effective Thermal Boundary Resistance
CVD: Chemical Vapor Deposition
SEM: Scanning electron microscope
CW: Continuous Wave
HF: Hot Filament
MW: Microwave

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