Improvements in the Annealing of Ion Implanted III-Nitride Materials and Related Devices

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Abstract

The activation of ion implanted p-type dopants in GaN is notoriously difficult as the extremely high temperatures required to activate implanted Mg also damage the GaN crystal. In this work, we present refinements to our novel annealing process (symmetric multicycle rapid thermal annealing, SMRTA) and apply the technique to Mg-implanted bulk GaN to realize rectifying junctions. The process demonstrated here represents a key enabling step for future GaN-based power devices.

INTRODUCTION

The GaN-based materials system has attracted significant interest due to the wide range of applications, including optoelectronic devices, high speed and power devices, and devices for operation in extreme environments. Unfortunately, the ability to implant and activate dopants in III-nitride materials is not well understood, and it is a key technical impediment to true planar processing in the III-nitride material system. Vertical power devices in particular, such as the current aperture vertical electron transistor (CAVET), Schottky diodes with guard ring termination or grayscale junction termination extension, and trench MOSFETs will be enhanced and enabled by the ability to selectively dope GaN without the need for etching or regrowth [1-4]. Here, we report on the development of a novel processing technique to achieve high efficiency activation of implanted dopants as well as characterize bulk GaN vertical p-i-n diodes fabricated using this technique.

EXPERIMENTAL

A 8 μm thick unintentionally doped GaN layer was grown by metal organic chemical vapor deposition (MOCVD) on a n^+ Ga-face c-oriented GaN substrate. The as-grown MOCVD film is smooth and exhibits step flow growth indicative of high quality epitaxial GaN. The p-GaN anode and termination regions were formed by Mg implantation to a concentration of $2x10^{19}$ cm^{-3} following a box profile to a depth of 500nm. A photoresist mask was used for the implantation, aligned to zero level marks etched 100nm into the GaN by Cl_2-based inductively coupled plasma (ICP) etching. The implanted dopants were activated using the symmetric multicycle rapid thermal annealing (SMRTA) technique described later. After activation by SMRTA to a maximum temperature of 1410 °C and removal of the sputtered AlN protective cap structure using AZ400K [5], The anode metal was formed by lift-off of Pd/Au (20/100nm), followed by rapid thermal annealing in a N_2 atmosphere, and the cathode metal was a blanket film of e-beam deposited Al on the back side of the sample. A schematic of the device structure is shown in Figure 1.

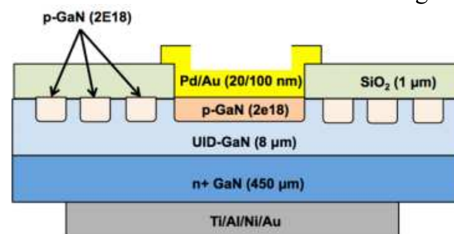

Figure 1. Device Cross Section

The activation of implanted dopants in GaN has two separate requirements. First, the damage created by the implantation must be reversed. Secondly, the implanted ions must be given enough energy to migrate to their proper lattice sites. In the case of Mg implanted GaN, the Mg must replace Ga to result in p-type material. In many other semiconductor materials such as Si and SiC, ion implantation is a routine step in most processing sequences. In GaN, the activation of implanted dopants is more difficult and has been the subject of intense research. This difficulty arises from the high temperatures to achieve p-type doping after implantation (>1300 ˚C). GaN begins to decompose at around 840 ˚C at atmospheric pressures, creating a gap of over 450 ˚C between the temperatures needed to activate p-type dopants and the decomposition temperature of GaN.

Several methods have been attempted to achieve the high temperature annealing of GaN while avoiding decomposition. One method is to utilize a high nitrogen overpressures (>10,000 bar), which has been successfully demonstrated as a method to achieve stability at temperatures up to 1500 ˚C [6]. However, the pressures required are prohibitively high and require specialized equipment that is not easily scalable. Alternatively, capping materials have also been shown to extend the range of decomposition in GaN.

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We have previously reported a process utilizing a combination of the two approaches, termed multicycle rapid thermal annealing (MRTA) [7]. In this research, we present an optimized annealing scheme termed symmetric multicycle rapid thermal annealing (SMRTA) as shown in Figure 2, which includes two conventional anneals performed at thermodynamically stable temperatures with rapid heating and cooling pulses sandwiched between in addition to an optimized capping structure [8]. Nomarski imaging was used to monitor the annealing process and qualitatively assess the reversal of implant damage, as shown in Figure 3. The crystal quality of the GaN before and after the annealing process was quantified using Raman spectroscopy mapping. It was determined that the FWHM of the GaN E_2 mode increases after the implantation process, consistent with crystalline damage, as shown in Figure 4.

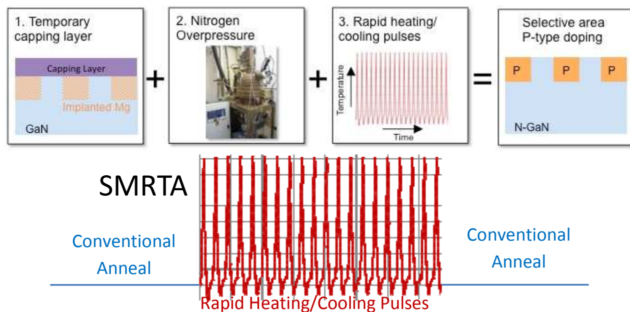

Figure 2. A schematic of the SMRTA process, which is composed of two conventional annealing steps with rapid heating and cooling pulses between the conventional annealing steps.

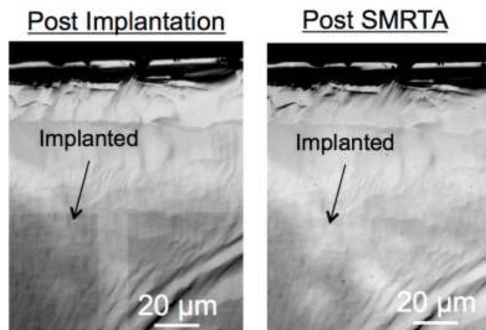

Figure 3. Nomarski images of selectively implanted structure

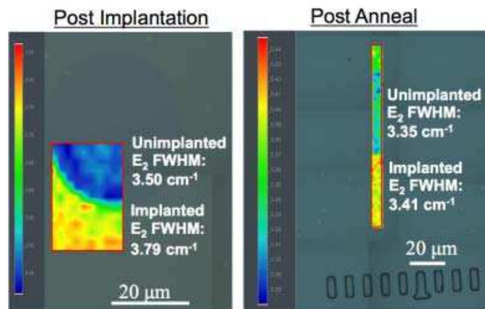

Figure 4. Raman map for the p-i-n structure after implantation and after SMRTA.

Upon optical inspection of the devices after capping for SMRTA, cracking was initially observed. Several problems arise in capping bulk GaN that are not present in capping heteroepitaxial GaN on sapphire films where the cap and SMRTA process was initially developed. First, both the front and back of the substrates need to be encapsulated to prevent GaN decomposition during SMRTA. Second, it was determined that cracking of AlN occurs on epi-ready face under elevated temperature sputtering conditions (T_{sub}= 400 ˚C). This cracking did not occur on heteroepitaxial surfaces that were rougher than the polished bulk GaN surfaces (i.e. optical polish). Cracking happens with both thick and thin sputtered AlN and is due to the lattice mismatch between GaN and AlN. The cracking was effectively mitigated by employing an optimized capping structure for bulk GaN samples using low temperature sputtered AlN [9].

RESULTS

Rectifying behavior was observed, as shown in Figure 5 for the device with the optimized cap. This represents a first for a p-i-n structure formed by Mg ion implantation in GaN. The turn-on voltage is consistent with a p-n junction, and the ideality factor of 2.6 is consistent with a recombination/generation-based transport mechanism. Non-ideal behavior is associated with recombination in the drift layer due to crystalline defects. The devices suffer from high ON-resistance due to high contact resistance and recombination in the drift layer, which limited the forward current to 1 A/cm^2. Capacitance-voltage measurements indicated the presence of a p-GaN layer, with a depletion layer thickness ~500nm and a doping density of 2x10^{18} cm^{-3}, corresponding to an activation ratio of 10%. The On/Off ratio at +/-10 V was 10^6.

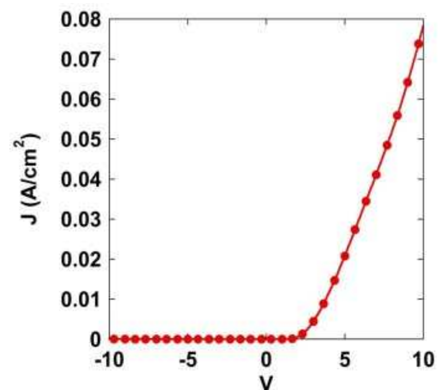

Figure 5. I-V curve of the vertical Mg-implanted GaN pin. The turn on voltage is around 3 V with an on/off ratio of over 10^6.

To further probe the nonideal diode behavior, we investigated the properties of the drift layer after processing. An AFM investigation of the surface after device processing indicated an increase in surface roughness from, 0.51 nm to 1.33 nm, as shown in Figure 6. This was traced to the capping process, which involved a 10W plasma clean prior to sputtering. As plasma damage in GaN is typically n-type,

this was identified as the source of high contact resistance due to type inversion. Modification to the process resulted in preservation of the smooth, stepped surface through the entire fabrication sequence, shown in the right frame of Figure 6.

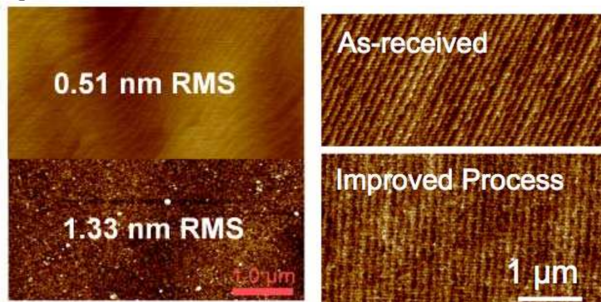

Figure 6. Atomic force microscope image of the GaN surface before (top) and after (bottom) a 10 W plasma clean used prior to the AlN cap deposition (left) , and after implementation of improved sputter process (right)

Blocking tests, indicate a breakdown voltage of ~300V based on a criteria of J=10 mA/cm^2. The breakdown voltage was independent of termination design, as shown in Figure 7. The optimized capping process significantly improved reverse leakage, further improving on/off ratio by several orders of magnitude However, the breakdown voltage was not improved and appears low for the thickness of the drift layer. This implies that either the background doping in the drift region is too high or the critical field is low due to damage from the ion implantation.

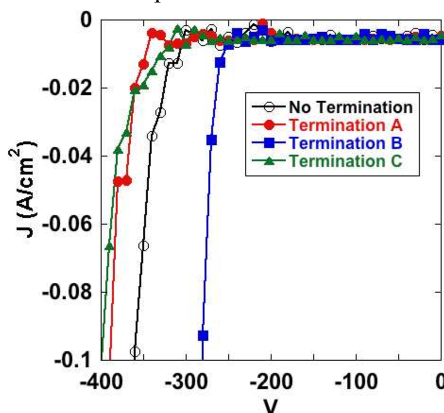

Figure 7. Blocking measurements on devices with and without optimized cap process

Electroluminescence (EL) imaging was used to further study the device behavior. The devices were stable over a period of hours while the images were being acquired, and emission began near the anode at low bias conditions and extended to increasing distances (>100um) at high bias conditions, as shown in Figure 8. The device with the unoptimized cap process exhibited a weak, nonuniform luminescence around the pad edge, indicting transport dominated by extended defects and non-radiative centers. In contrast, the device with the optimized cap process exhibited an intense luminescence around the pad edge, indicative of uniform high efficiency injection.

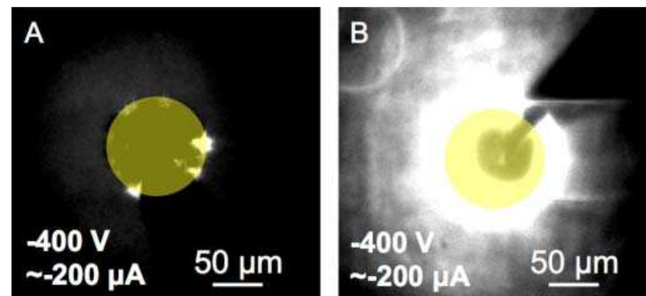

Figure 8. Broadband EL images of devices with unoptimized (A) and optimized (B) capping processes. The intensity scale is identical.

CONCLUSIONS

An ion implanted GaN p-i-n diode enabled by the symmetric multicycle rapid thermal annealing technique was demonstrated. The capping structure was optimized to avoid cracking of the AlN layer as well as eliminate plasma damage to the GaN surface. Electrical characterization exhibited rectifying behavior with low reverse leakage current and forward characteristics consistent with a GaN p-n junction. The breakdown voltage is still low due to either high background doping in the drift region or a low critical field due to a defective GaN layer near the junction and possibly in the depletion region. The ability to integrate p-type GaN layers in planar device structures by ion implantation represents a significant step for next-generation power devices.

ACKNOWLEDGEMENTS

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