Compatibility of AlN/SiN_x Passivation Technique with High-Temperature Process

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Abstract

In this work, we demonstrate an integrated process that illustrates the compatibility of AlN/SiN_x passivation with a high temperature process, i.e. low-pressure chemical vapor deposition (LPCVD) of SiN_x gate dielectric at 780 °C for GaN-based MIS-HEMT. The LPCVD-SiNx exhibits many benefits including low leakage, high breakdown and high time-dependent-dielectric breakdown (TDDB). It is shown that the AlN/SiN_x passivation structure maintains its superior capability of suppressing the current collapse after undergoing high temperature of 780 °C during the LPCVD-SiN_x deposition. AlN/SiN_x passivation is shown to be superior to LPCVD-SiN_x passivation by delivering small dynamic R_{ON} degradation, especially under high drain bias switching with V_{DS} > 100 V and after ON-state drain biased stress.

INTRODUCTION

Gallium Nitride-based high-electron-mobility transistors (HEMTs) and metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) are capable of delivering superior performance in high-frequency power amplifiers and high-voltage power switches [1]. Compared to the conventional Schottky gate HEMTs, MIS-HEMTs are highly preferred for high-voltage power switches, due to the suppressed gate leakage and enlarged gate swing. To obtain stable and reliable GaN power MIS-HEMTs, it is essential to develop a process that allows simultaneous optimization of gate dielectric and passivation layer.

Recently, the low-pressure chemical vapor deposition (LPCVD) silicon nitride, which has been widely used in the CMOS process, has been shown to exhibit superior properties (especially in dielectric breakdown) for GaN-based MIS-HEMTs [2, 3]. Compared to a wide range of gate dielectrics prepared by atomic layer deposition (ALD) and plasma enhanced chemical vapor deposition (PECVD) that feature process temperature in the range of 300~400 °C, LPCVD-SiN_x offers clear advantages in lower leakage and higher breakdown [2], primarily because of reduced defects enabled by higher deposition temperature (e.g. 780 °C) and suppressed oxygen contamination. However, as a passivation layer [4, 5], the effectiveness of LPCVD-SiN_x to suppress current collapse in the pulsed *I-V* tests has only been confirmed at low drain bias smaller than 100 V [6].

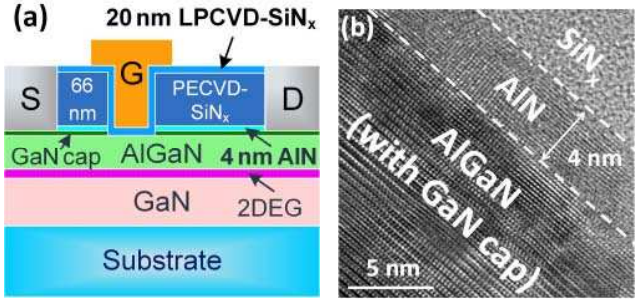

Fig. 1. (a) Schematic cross-sectional view of the GaN-based MIS-HEMTs with LPCVD-SiN_x gate dielectric and PEALD-AlN/PECVD-SiN_x passivation. (b) Cross-sectional TEM micrograph of the passivation stack in access region.

Another passivation structure based on surface trap compensation by polarization charges has been demonstrated with an AlN/SiN_x stack, in which the monocrystal-like polarized AlN epitaxial film is deposited by plasma enhanced atomic layer deposition (PEALD) at 300 °C and the SiN_x is deposited by PECVD at 300 °C [7, 8]. This passivation has been shown to deliver effective current collapse suppression at high drain bias stress and high temperatures under both soft- and hard-switching operations. Since bare amorphous AlN thin films have been shown to form polycrystalline grains through partial crystallization at temperature > 500 °C [9], the compatibility of the AlN/SiN_x passivation technology with high temperature process such as LPCVD is of major concern, and no related work has been reported to date.

In this work, we integrate the AlN/SiN_x passivation with the LPCVD-SiN_x gate dielectric to simultaneously obtain low gate leakage, high gate breakdown and low current collapse in high-voltage AlGaN/GaN MIS-HEMT. It is shown that the AlN/SiN_x passivation after undergoing high temperature process at 780 °C can still suppress the surface-state-induced effects efficiently, validating the compatibility of AlN/SiN_x passivation with high-temperature process.

DEVICE FABRICATION

The MIS-HEMT devices were fabricated on an AlGaN/GaN heterostructure sample, grown by MOCVD on a

p-type Si (111) substrate. The epi-structure consists of a 2 nm undoped GaN cap layer, a 20 nm AlGaN barrier, a 1 nm AlN interface enhancement layer and a 4 µm GaN buffer/transition layer. The cross-sectional schematic of the device structure is depicted in Fig. 1 (a).

The device fabrication commenced with remote plasma pretreatment (RPP) in a plasma-enhanced atomic layer deposition (PEALD) system to remove the surface native oxide on sample with minimum surface damage [10]. Then a 4 nm PEALD-AlN layer was deposited *in-situ*, immediately followed by the deposition of a 66 nm silicon nitride layer using PECVD. The PEALD-AlN was deposited at 300 °C, using N_2, and trimethylaluminum (TMA) plasma precursors as the N and Al sources. The PECVD-SiN_x was deposited at a base-plate temperature of 300 °C. Then, the gate window was opened by inductively coupled plasma (ICP) reactive ion etching of the PECVD-SiN_x layer and removal of the PEALD-AlN. The remaining process steps are the same as those reported in ref. [2].

As the silicon nitride layer (20 nm) was deposited as gate dielectric by LPCVD at a high temperature of 780 °C, the AlN was inevitably annealed during the deposition process. To investigate the effects of the annealing on AlN, material characterizations and TLM measurement were conducted. According to the high-resolution TEM image in Fig. 1 (b), the interface between PEALD-AlN and GaN cap was still of high quality as an atomically sharp interface was observed, indicating that the PEALD-AlN can maintain its crystalline structures at high temperatures when it is capped by PECVD-SiN_x. It is experimentally confirmed that a bare 4 nm AlN film without the SiN_x cap started to crystallize at 500 °C. The thermally stable SiN_x cap layer is responsible for maintaining the integrity of the AlN thin film by providing tensile stress. Confirmed by the XPS spectra of Ga 3d core level, the Ga-O bonds at the AlN/GaN cap interface, which are detrimental to the interface quality, are not increased after annealing. Measured by TLM, the sheet resistance of the 2DEG channel was 262 Ω/sq, which is the same as that of the 2DEG channel covered by the AlN/SiN_x passivation without undergoing high temperature process [7]. The strain relaxation of the AlGaN barrier induced by the high temperature process is about 2%, as confirmed by high- resolution XRD measurement.

For comparison, MIS-HEMTs with 70 nm LPCVD-SiN_x passivation layer and 20 nm LPCVD-SiN_x gate dielectric were also fabricated.

CHARACTERIZATION AND ANALYSIS

Both the MIS-HEMTs with AlN/SiN_x passivation or LPCVD-SiN_x passivation exhibit a threshold voltage (V_{TH}) of -11.5 V by linear extraction, a small sub-threshold swing of ~ 70 mV/dec and a high I_{ON}/I_{OFF} ratio in the order of ~ 10^8 at V_{DS} = 1 V (Fig. 2 (a)). In particular, a small hysteresis (ΔV_{TH}) of ~ 0.08 V was observed between the up- and down-sweep transfer curves with a sweeping rate of 0.7 V/s, indicating the high quality of dielectric/barrier interface. The gate leakage was almost identical for the MIS-HEMTs with different passivation layers (Fig. 2 (b)), suggesting the AlN/SiN_x passivation technology has no adverse effects on the performance of LPCVD-SiN_x gate dielectric. Due to the effective suppression of gate leakage by the gate dielectric, both the AlN/SiN_x passivated and LPCVD-SiN_x passivated MIS-HEMTs deliver a high OFF-state breakdown voltage of 690 V at drain leakage current of 1 µA/mm, which was dominated by the vertical substrate leakage through the buffer.

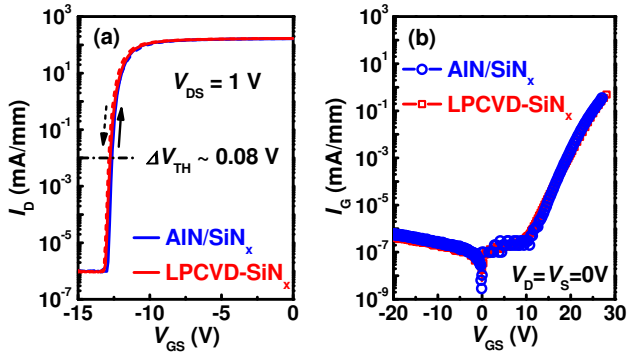

Fig. 2. (a) Transfer characteristics and (b) gate leakage characteristics of LPCVD-SiN_x/AlGaN/GaN MIS-HEMTs with LPCVD-SiN_x passivation and AlN/SiN_x passivation. Device dimensions: $L_G/L_{GS}/L_{GD}$ = 1.5/2/15 µm.

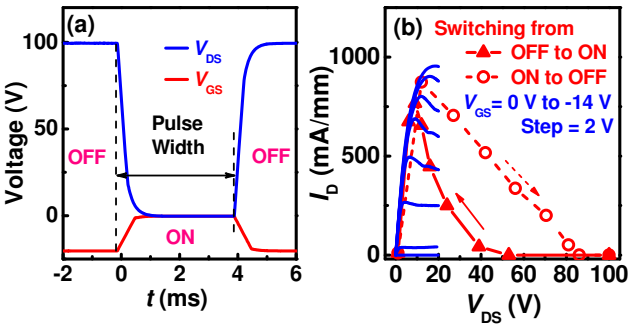

Fig. 3. (a) Waveforms of V_{GS} and V_{DS} during the hard-switching test and (b) estimated load line during the hard switch from ON state to OFF state and from OFF state to ON state.

Hard-switching double-pulsed I_D–V_{DS} characteristics were measured to evaluate the effectiveness of passivation, namely, the suppression of current collapse. The waveforms of gate bias and drain bias were shown in Fig. 3 (a). The pulse width and pulse period are 4 ms and 20 ms. The output curves were measured with quiescent bias points set at (V_{GSQ}, V_{DSQ}) = (-15 V, 0 V), (-15 V, 50 V), (-15 V, 100 V) and (-15 V, 200 V), respectively. The V_{DSQ} was limited to 200 V due to the transient high power and high current during the hard switching shown as the load line in Fig. 3 (b). The pulsed output characteristics of the AlN/SiN_x-passivated MIS-HEMTs were shown in Fig. 4 (a) and the DC output curves were plotted for reference. The effective suppression of current collapse by AlN/SiN_x passivation is demonstrated with little difference between the dc and pulsed drain current

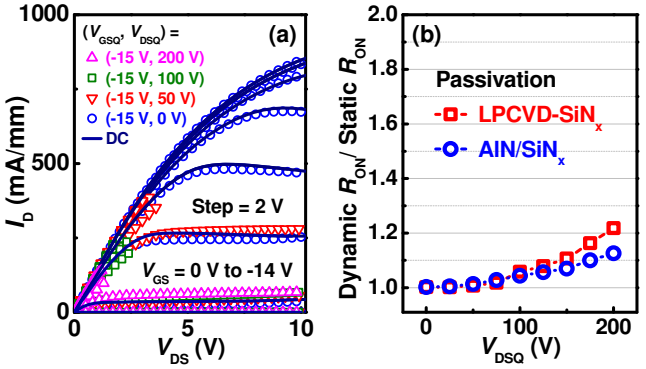

Fig. 4. (a) DC and pulsed output characteristics of MIS-HEMT with AlN/SiN_x passivation. (b) Dynamic R_{ON} of MIS-HEMT with LPCVD-SiN_x passivation and that with AlN/SiN_x passivation. Device dimensions: $L_G/L_{GS}/L_{GD}$ = 1.5/2/15 μm.

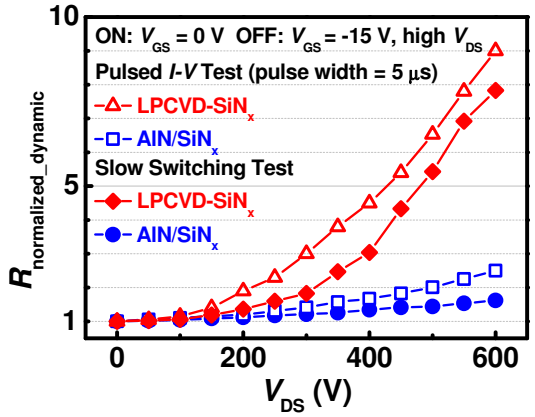

Fig. 5. Dynamic R_{ON} of MIS-HEMTs with LPCVD-SiN_x or AlN/SiN_x passivation measured by slow switching test and pulsed I-V test. Device dimensions: $L_G/L_{GS}/L_{GD}$ = 1.5/2/15 μm.

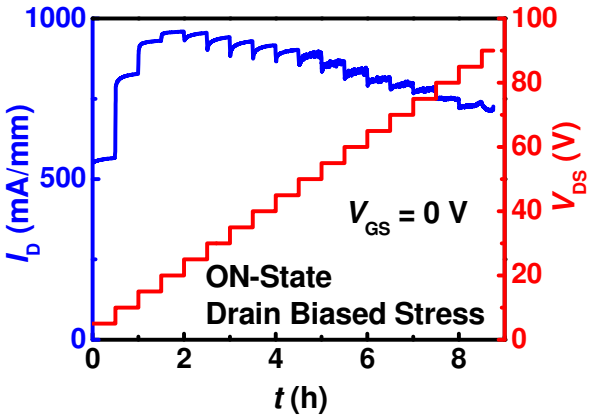

Fig. 6. Drain current I_D and bias V_{DS} of MIS-HEMT with AlN/SiN_x passivation during on-state drain biased stress with V_{GS} = 0 V. Device dimensions: $L_G/L_{GS}/L_{GD}$ = 1.5/2/15 μm.

in the linear region (Fig. 4 (a)). Compared with the LPCVD-SiN_x passivation, the AlN/SiN_x shows an enhanced dynamic performance with V_{DSQ} higher than 100 V (Fig. 4 (b)).

To evaluate the dynamic performance of the MIS-HEMTs at higher drain voltage, the dynamic ON-resistance was measured under soft-switching conditions (i.e. V_{DS} is set to zero from OFF-state drain bias before biasing the device to ON-state). Both high-voltage slow switching test and pulsed I-V test were conducted.

In the high-voltage slow switching test, the device was switched to ON-state from various OFF-state drain bias V_{DS} (from 0 V to 600 V with a step of 50 V) within 1.5 s as described in [11]. As shown in Fig. 5, the two passivation schemes (i.e. AlN/SiN_x and LPCVD-SiN_x) yield similar dynamic ON-resistance (R_{ON}) for drain bias smaller than 100 V, but start to exhibit large differences as V_{DS} exceeds 100 V. With a V_{DS} stress at 600 V, the normalized dynamic R_{ON} (defined as the ratio, dynamic R_{ON}/static R_{ON}) is only 1.61 with AlN/SiN_x passivation that has undergone high temperature process, which is similar with AlN/SiN_x passivation without undergoing high temperature annealing [7], but is significantly larger at 7.8 with LPCVD-SiN_x passivation.

The pulsed I-V test was performed with an AMCAD AM241 pulsed I-V system. The pulse width and period were 5 µs and 100 µs, respectively. The drain bias was dropped to zero from the OFF state (with a gate bias V_{GSQ} = -15 V) before biasing the device to ON state, defined at V_{GS} = 0 V. The transient ON-state drain current I_D was sampled 2 µs after each OFF-to-ON switching event. Dynamic R_{ON} was extracted from the linear region of the pulsed output curve. Under the high-speed switching conditions, the AlN/SiN_x passivation still delivers much smaller dynamic R_{ON} degradation (2.5 @ V_{DSQ} = 600 V) than the LPCVD-SiN_x passivation (9 @ V_{DSQ} = 600 V) when V_{DSQ} exceeds 100 V.

The large difference of dynamic R_{ON} degradation at high drain bias stress stems from the difference in the mechanisms of the two passivation schemes. The AlN passivation is based on the high-density positive polarization charges (which are fixed) in epitaxial AlN thin film [12], while the SiN_x passivation is based on the high-density shallow donors (whose charge state can be changed by time-dependent trapping/de-trapping processes) introduced at the SiN_x/GaN interface [13].

The reliability of the LPCVD-SiN_x gate dielectric has been evaluated by the TDDB tests as reported in ref. [3]. To evaluate the reliability of the AlN/SiN_x and LPCVD-SiN_x passivation, ON-state drain bias stress was performed. The ON-state stress occurring in prolonged device operation under hard-switching conditions was reported to cause the formation of shallow traps inside the barrier or at its surface, resulting in R_{ON} degradation [14]. To conduct the ON-state drain biased stress, the MIS-HEMTs were stressed at V_{GS} = 0 V. The drain bias V_{DS} swept from 0 V to 85 V with a step of 5 V and a duration of 30 min for each step (Fig. 6). After each step of stress, output characteristics were measured with V_{GS} = 0 V and V_{DS} swept from 0 V to 3 V to estimate the ON-resistance. Then the dynamic performance was also evaluated by slow switching test with OFF-state drain bias V_{DS} = 200 V.

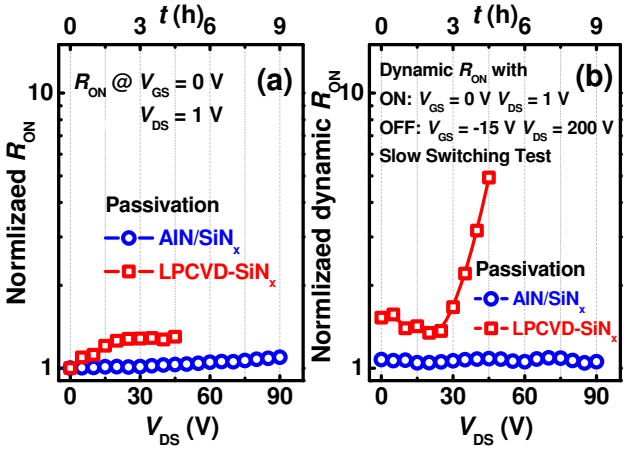

Fig. 7. (a) Normalized R_{ON} and (b) normalized dynamic R_{ON} measured by slow switching test with off-state V_{DS} = 200 V after each step of 30-min ON-state drain biased stress.

For the MIS-HEMT with LPCVD-SiN$_x$ passivation, the gate leakage increased suddenly during stress at V_{DS} = 50 V and permanent degradation of R_{ON} was observed. On the other hand, the MIS-HEMT with AlN/SiN$_x$ passivation exhibits much smaller R_{ON} degradation (Fig. 7(a)), indicating a robust AlN/barrier-layer interface and the well-maintained polarization charges in AlN after enduring the ON-state stress. As shown in Fig. 7 (b), the dynamic performance of the AlN/SiN$_x$ passivation delivers no degradation even after ON-state stress with V_{DS} = 85 V for 30 min, while the dynamic performance of LPCVD-SiN$_x$ passivation exhibits obviously degradation after stress with V_{DS} = 35 V.

CONCLUSIONS

The AlN/SiN$_x$ passivation technique has been demonstrated to be compatible with the high-performance LPCVD-SiN$_x$ gate dielectric. The LPCVD-SiN$_x$ MIS-HEMT with AlN/SiN$_x$ passivation delivers robust gate dielectric and effective suppression of current collapse. The AlN/SiN$_x$ passivation after enduring high-temperature of 780 °C during the LPCVD-SiN$_x$ deposition can still suppress the current collapse effectively, confirming the compatibility of the passivation technology with high temperature process.

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ACRONYMS

HEMT: High-Electron-Mobility Transistors
MIS-HEMT: Metal-Insulator-Semiconductor High-Electron-Mobility Transistors
LPCVD: Low-Pressure Chemical Vapor Deposition
PECVD: Plasma-Enhanced Chemical Vapor Deposition
PEALD: Plasma-Enhanced Atomic Layer Deposition
TLM: transfer length method