Simulation of Fabrication- and Operation-Induced Mechanical Stress in AlGaN/GaN Transistors

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Abstract

Mechanical stress is an important factor influencing the performance and reliability of GaN based devices. In this work, mechanical stress resulting from fabrication and operation of AlGaN/GaN transistors has been modelled using a finite element analysis approach. Specifically, this study compares SiN induced mechanical stress for devices of different architectures. Thermal and inverse piezoelectric stresses resulting from device operation, as well as the effect of source field plates on mechanical stress in AlGaN/GaN devices, is also investigated. Finally, the potential impact of mechanical stress on device reliability is discussed.

INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMTs) are among the leading candidates of devices for next generation RF microwave and power electronics. Mechanical stress plays an important role in the performance and reliability of these devices, due to the highly polar and piezo-electric nature of III-N semiconductors [1, 2]. Device-fabrication-related parameters such as the intrinsic stress of SiN films and the proximity of various contact regions can influence the magnitude of the localized mechanical stress in these devices. In addition, high voltages and temperature gradients associated with device operation can induce additional mechanical stresses. These stresses are usually concentrated in small regions near the drain-side edge of the gate [3], and may lead to reliability concerns such as pit/crack-type defects, trap generation, and enhanced impurity diffusion [4]. Hence, in this work, a finite element modelling approach has been used to obtain mechanical stress values in AlGaN/GaN, with a view to understand its impact on device performance and reliability.

APPROACH

The device structures simulated in this work are typical AlGaN/GaN HEMTs with 0.5-µm gate length. The devices have a layer of surface passivation SiN (SiN-1) and the gate is defined by etching an aperture in SiN-1 followed by gate metal deposition. The gate metal is larger than the SiN-1 aperture creating gate field plates (GFP). A second layer of SiN (SiN-2) is then deposited followed by fabricating metal interconnects which also create source field plates (SFP).

ANSYS 15.0 was used to simulate temperature and mechanical stress in AlGaN/GaN HEMTs. For all mechanical stress simulations, the bottom surface of the model was assumed fixed in the vertical direction. Symmetry conditions were used wherever applicable to reduce computation time. All metals in the structure (ohmic and gate contacts) were approximated to be pure gold.

Mechanical properties of various materials were taken from relevant references- (Al)GaN [2], Gold [2], SiC [5], and Si [6]. Thermal properties of GaN, SiC, and Si, were taken from ref [7], [8], and [9], respectively. Temperature-dependent thermal conductivities were assumed for all materials.

RESULTS & DISCUSSION

1. Intrinsic SiN Stress and Device Layout

A key step in the fabrication process of a typical AlGaN/GaN HEMT is SiN deposition. Fig. 1 is a schematic of the structure simulated in this section. The SiN-1 film considered is 100 nm thick and has an intrinsic stress of around ~ 300 MPa in the biaxial direction, as obtained from curvature measurements on 4'' silicon wafers. Throughout this paper, biaxial stress is defined as the mechanical stress along the direction parallel to the current flow in the device (along x direction in Fig. 1). The gate length, SiN and GaN thicknesses are 0.5, 0.1 and 2 µm respectively. The gate foot (i.e. the bottom corner of the gate aperture) to ohmic contact spacing *L* is varied. The sidewall of the gate in contact with the SiN layer is assumed to be at an angle of 45° to the GaN

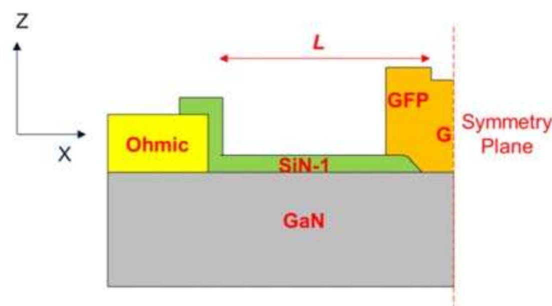

Figure 1. Schematic of simulated structure.

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surface. In addition, the corner between the GFP and the SiN is given a small fillet of radius 100 nm, representative of a real device. Although the intrinsic stress in the SiN film is ~ 300 MPa, the stress in the GaN due to the SiN stress will be much higher near the corner of the gate. Fig. 2 shows the distribution of stress for the case of L = 3 μm. In the vicinity of the ohmic contact, the stress field is compressive, because of the large thermal coefficient difference between standard ohmic metals and GaN. While gold was chosen here as the ohmic metal for the purpose of simulation, Ti, Al and Ni also have thermal expansion coefficients higher than GaN and would lead to a compressive stress field near the contact as well. However, near the gate edge, the stress field is tensile due to the concentration of tensile stress at the corner

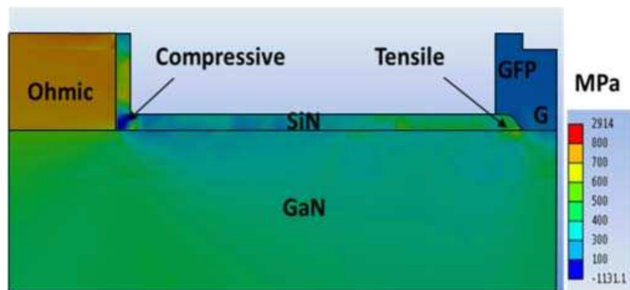

Figure 2. Stress distribution due to the SiN intrinsic stress

between the GaN, gate and SiN. As the ohmic-gate spacing L reduces, the interaction of these two stress fields changes the stress distribution in the GaN. As seen in Fig. 3, at an ohmic-Schottky contact spacing of L = 3 μm, the stress in the GaN is maximum at the gate corner and is almost double (~ 600 MPa) the intrinsic SiN stress. However, as L reduces to 0.5 μm, the compressive stress field from the ohmic region dominates and the overall stress in the GaN is compressive. Similarly, the stress in the SiN is reduced to ~ 43 MPa.

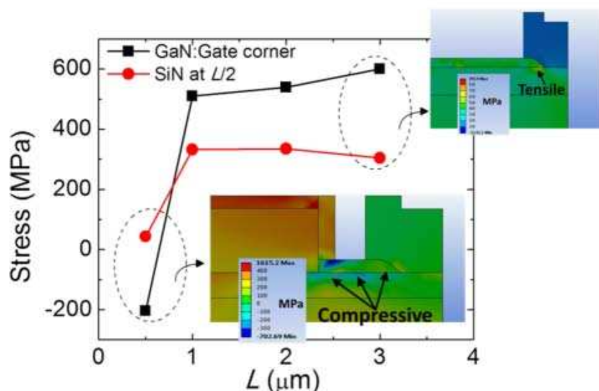

Figure 3. Variation of biaxial stress in the GaN at the gate corner and the SiN with ohmic-schottky contact spacing.

While it is to be noted that the exact nature of the stress field in the ohmic region has not been modeled (due to the complex processes involved in formation of alloyed contacts), it can be concluded that as the ohmic-gate spacing reduces, the stress fields from the ohmic contact starts to influence the entire region between the gate and the ohmic contact.

2. Thermal Stress during Device Operation

Current flow in AlGaN/GaN devices causes heat generation due to Joule heating. The resulting temperature gradients generate thermally induced mechanical stress in these devices. Fig. 4 (a) shows the schematic of the structure simulated.

Heat generation in the device was simulated by assuming a uniform heat flux spread over a length of 0.4 μm near the source field plate, which corresponds to the location of the maximum power density during operation. The thermally generated stress in the AlGaN/GaN is of a compressive nature. But the stress in a small region near the drain side edge of the gate is under tensile stress, as shown in Fig. 4 (b). Hereafter, this region will be referred to as 'the junction'. This thermally generated stress will add to the tensile stress at the junction leading to reliability concerns.

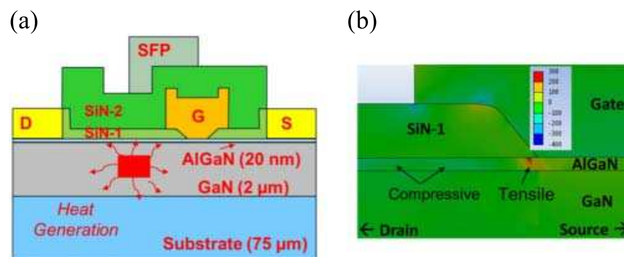

Figure 4. (a) Schematic of simulated structure showing the location of the heat generation region. (b) Stress map showing tensile stress near the drain-side corner of the gate.

2.1 Effect of Source Field Plate

SFPs are typically introduced in devices in order to spread the peak electric field near the gate, increasing device breakdown voltage and reducing DC-RF dispersion. As a result, the peak power density during operation is shifted away from the gate region and the total power is spread over a larger area enabling better power dissipation. As shown in Fig. 5, another advantage of SFPs is the reduction of the tensile stress at the junction. For a high power density of 10W/mm, the presence of the SFP and the additional SiN-2 layer reduces the tensile stress from 457 to 309 MPa. This reduction is because of two reasons – (a) the presence of the SFP shifts the maximum power density region away from the gate. This results in the heat flux region used in our simulations to move away from the gate region, resulting in a lower temperature near the gate. (b) The presence of the additional layers (SiN-2 and SFP) shifts the free surface (where vertical stress is zero) away from the gate region, resulting in a stress distribution which lowers the tensile stress.

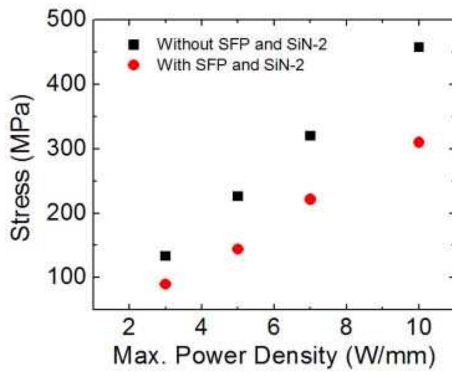

Figure 5. Comparison of tensile stress at drain-side corner of gate for devices with and without SFP and SiN-2. The substrate was considered to be SiC.

A uniform power distribution was assumed to get the result shown in Fig. 5. It is worth mentioning that a non-uniform distribution (assuming a triangle shape) was also simulated and no obvious difference was observed. The total power density and the distance of the heat source from the junction are the most important factors determining mechanical stress.

2.2 Thermal Stress and Peak Temperature

In accelerated lifetime test (ALT), device peak temperature at the junction is varied normally by changing base temperature while maintaining constant electrical power dissipation. The thermal properties of the substrate on which AlGaN/GaN is hetero-epitaxially grown have significant influence on the thermal gradient in the active device region and the resulted mechanical stress. The biaxial stress is proportional to the horizontal temperature gradient (dT/dx). ANSYS thermal simulations were done to obtain the peak temperature.

Fig. 6 (a) shows the stress at the junction as a function of

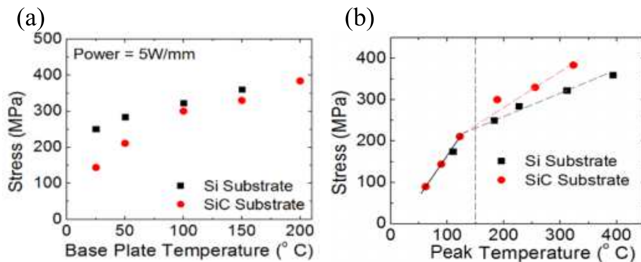

Figure 6. (a) Stress at the junction vs. base plate temperature (b) Stress at the junction vs peak temperature.

the base plate temperature for GaN/SiC and GaN/Si, applied directly at the bottom of the substrate of the device structure shown in Fig. 4 (a). At low temperatures, the stress values are lower for GaN/SiC, because of the somewhat higher thermal conductivity of SiC over Si. However, as the temperature increases, the difference in mechanical stress for the two different substrates decreases. This is because with increasing temperatures, the thermal conductivity of SiC drops faster and converges to that of Si.

Fig. 6 (b) shows the same tensile stress shown in Fig. 6 (a), but plotted against the peak temperature. Since we are considering only mechanical stresses imposed due to thermal gradients, for the same peak temperature, the stress is expected to be the same for both Si and SiC substrates. At low peak temperatures (< ~150 º C), this is indeed the case. However as the temperature increases, slightly lower stress values are obtained for the GaN/Si devices. Moreover, the stress increases less rapidly with temperature, as seen by the change in slope at higher peak temperatures. These results can be explained as follows.

The horizontal temperature gradient (dT/dx) is proportional to the peak temperature T. However, at higher temperature, the thermal conductivity k of AlGaN is known to increase [10], which requires that (dT/dx) reduce in order to keep constant flux($q = -k(\frac{dT}{dx})$). These competing contributions to (dT/dx) result in a slower rate of increase of (dT/dx) with temperature, causing the slope of stress vs. temperature to reduce.

The stress in the GaN/Si structure is slightly smaller. This can be explained by the fact that for similar peak temperature, the base plate temperature applied is lower for GaN/Si than for GaN/SiC. This leads to a higher vertical thermal gradient dT/dz (from the base plate to the device region), giving a slightly smaller biaxial stress near the junction due to the Poisson ratio effect. It can thus be concluded that for different substrates, the same peak temperature does not imply the same tensile stress at the gate junction.

3. Inverse Piezo-electric Stress

In GaN based devices, large voltages applied induce mechanical stress due to the inverse piezo-electric effect [11]. An analytical calculation was performed to obtain the values of mechanical stress imposed due to typical drain to gate voltages applied in the device shown in Fig. 4(a). For typical operating drain to gate voltages of 50V, the maximum mechanical stress was calculated to be ~ 300 MPa. This maximum also occurs at the junction region described above, as this is also the location of the maximum electric field along the channel, under normal bias conditions.

4. Cumulative Stress and Reliability

In AlGaN/GaN devices, lattice mismatch between the AlGaN barrier and the GaN layer causes a tensile stress in the biaxial direction. In addition, residual stresses resulting from the high temperature growth of GaN on different substrates are present. During device fabrication, stresses due to SiN passivation layers, proximity of contacts etc. are added, as discussed in Section 1. Under operation, thermal and inverse piezo-electric effect induced stresses are present,

particularly near the junction region as described in sections 2 and 3. Table 1 compares the various stress values for a typical device shown in Fig. 4(a). The residual and lattice stresses were obtained from ref. 3. From table I, it can be seen that the total stress due to the SiN passivation, thermal conditions and inverse piezo-electric effect is a significant fraction of the residual and lattice stresses (35 % in GaN on Si and 44 % in GaN on SiC). Although the stresses considered here are small compared with the yield strength of GaN (~10-15 GPa) [12] and SiN (2.4 GPa) at room temperature, they may still induce mechanical failure in regions of pre-existing defects such as dislocations. It should be noted that the thermally generated stress under on-state operation is comparable to the inverse piezo-electric stress. While it has been reported that the inverse piezo-electric effect could be an important device degradation cause [11], the thermally induced stress should be taken into account as well in assessing device reliability. In addition, impurity diffusion is known to be enhanced by mechanical stress**.** This is of concern, particularly in the junction region, where Ni from the gate metal stack can diffuse into the AlGaN/GaN layers, causing potential reliability issues [4]. As a result, in addition to the electric field engineering approaches developed for controlling the electric field distribution in the gate region, mechanical stress must also be carefully engineered in GaN based devices in order to improve reliability.

Table I.
Comparison of different stresses in GaN devices.

Stress	GaN on Si	GaN on SiC
Residual + Lattice	~ 3600 MPa	~ 2900 MPa
SiN passivation induced	600 MPa	600 MPa
Thermally generated stress	360 MPa	384 MPa
Inverse piezo-electric stress	~ 300 MPa	~ 300 MPa

CONCLUSIONS

AlGaN/GaN HEMTs of industry-typical architectures have been studied from a mechanical stress point of view in this work. The impact of the SiN film stress on the device structure has been simulated. Further, the thermal and inverse piezoelectric stress conditions were also simulated to consider practical device operation conditions. It was found that mechanical stress due to fabrication and device operation is not negligible compared with the residual and lattice stresses. While the stresses calculated are much less compared with the failure strength of materials such as GaN and SiN, they may be high enough to cause failure in regions with lattice defects such as voids or dislocations. It can be concluded that mechanical stress, induced by operation conditions as well as device fabrication, has the potential to play a role in device degradation, and should be considered in device design.

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ACRONYMS

HEMT: High Electron Mobility Transistor
GFP: Gate Field Plate
SFP: Source Field Plate
ALT: Accelerated Lifetime Test