

Uniformity Improvement and Defect Reduction of NiCr Thin Film Resistor

Chang'e Weng, Jinhong Yang, Ron Herring, Don Hamilton, Kaushik Vaidyanathan,
Brian Zevenbergen, Fred Pool, and Jeremy Middleton

Qorvo, 2300 NE Brookwood Parkway, Hillsboro, OR 97124
e-mail: Change.Weng@Qorvo.com, Phone: 503-615-9820

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Abstract

An optimized NiCr thin film resistor process has been developed using DC sputtering. NiCr uniformity has been improved by optimizing PVD shield size and height, and can be fine-tuned through wafer position adjustment. NiCr defects have been reduced by PVD shield modification, target burning, post liftoff cleans, and the staging time control before passivation.

INTRODUCTION

NiCr thin film resistor is the most commonly used resistor technology in GaAs IC design due to its advantages for producing high resistivity and low temperature coefficient of resistance¹. By optimizing process parameters, stable film properties including crystal structure and composition can be produced by using sputtering deposition technique. Therefore NiCr resistors could provide high stability of electrical properties². However, depending on the layout design and other process factors, NiCr film resistor electrical properties can be very sensitive. Within-wafer sheet resistance uniformity control and defect issues have always been challenging in high volume manufacturing. In telecommunication applications, typical NiCr resistors target a sheet resistance at 50 Ω /sq. NiCr film sheet resistance is highly sensitive to pre and post deposition cleans, substrate types and surface roughness. Within-wafer uniformity is critical for die yield and device performance, but is very difficult to control due to deposition tool limitations. In this paper we demonstrated the sputter deposition shield effect on within-wafer film uniformity. Different shield designs had significant impact on die yield and device performance. Moreover, optimizing NiCr film deposition power could reduce within-wafer sheet resistance standard deviation by 50%. A very tight sheet resistance spec window was achieved for all NiCr process flows of difference technologies. A novel approach for uniformity fine tuning by wafer position adjustment was also introduced in this paper and within-wafer uniformity can reach <1% using this approach.

Particle issue introduced during NiCr sputtering and post deposition process is another cause of die yield loss and unstable resistor electrical properties. In this paper, by continuously improving sputter target burn-in process, post

lift dry process and monitoring queue time before passivation, we identified and eliminated the sources of different types of NiCr particles and liftoff residues.

RESULTS AND DISCUSSION

NiCr Film Uniformity Improvement

In this work, NiCr thin film were sputtered on 150 mm GaAs wafers with an insulating oxide or nitride layer. Sheet resistance measurements were performed on van der Pauw structures as shown in Figure 1.

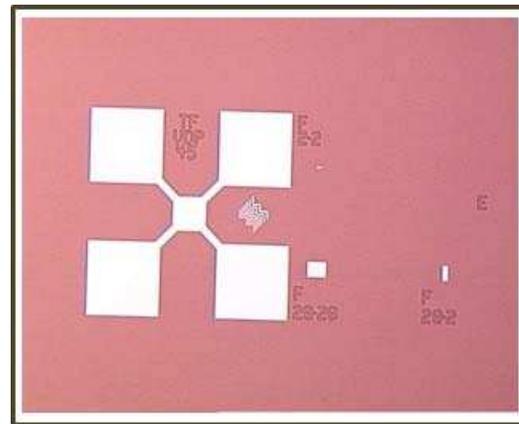


Figure 1. Van der Pauw structure for NiCr resistor sheet resistance measurements.

In a previous work we demonstrated effect of target power on within-wafer film uniformity.² Continuous work to study NiCr sheet resistance at low power range shows within-wafer uniformity can be further improved. Figure 2 shows the plot of sheet resistance measured on van der Pauw structures by using different deposition powers at lower power range. We reduced the NiCr resistance standard deviation by 50% from process A to process C.

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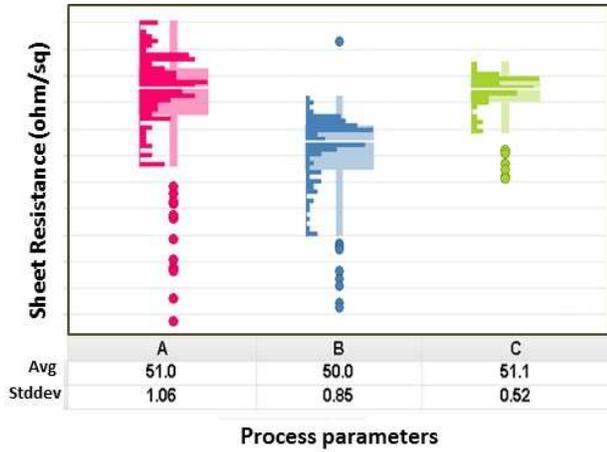
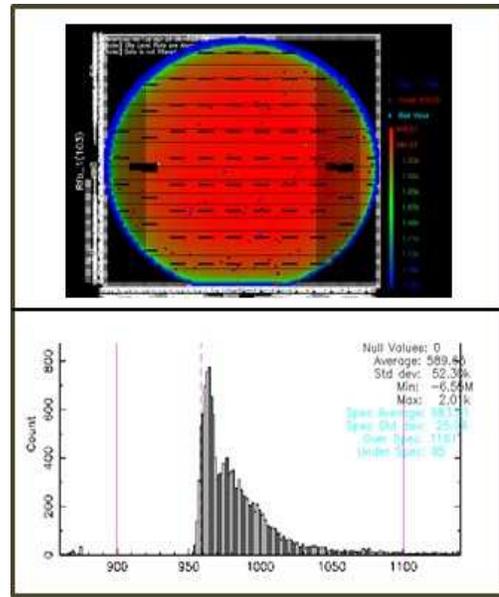


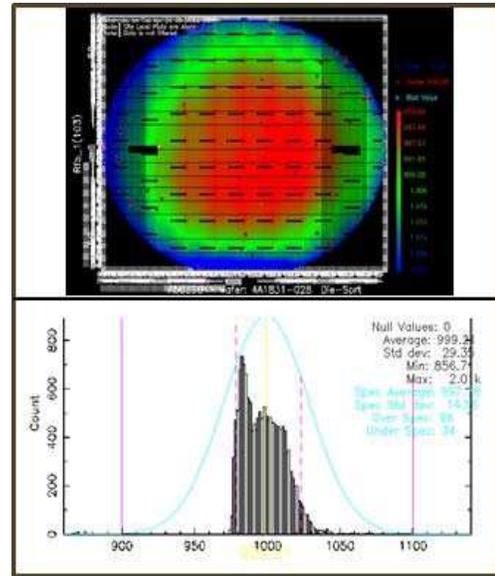
Figure 2. NiCr resistor sheet resistance at different process parameters.

As a common issue for sputter deposition, NiCr films usually exhibit higher sheet resistance at the wafer edge due to shield shadow effect. As shown in Figure 3(a) die sort wafer map, a higher resistance value was measured at the wafer edge. This particular resistor value shows a tail extending to the upper spec limit instead of a normal distribution. This caused die yield below 93%. To resolve this issue, different shield designs have been studied and we found that they had a significant impact to within-wafer uniformity of NiCr resistors. Die yield reached above 99% using a specially designed sputter shield. As shown in Figure 3 (b), a tighter distribution of resistor value was obtained with ~45% standard deviation reduction.

A fine tuning approach was developed for NiCr resistor sensitive masks. With optimized process power, shield design, NiCr resistor sheet resistance across an entire wafer can be further fine-tuned. Figure 4 (a) shows NiCr film sheet resistance at different locations of a wafer in relative to different wafer position inside of a chamber. For a NiCr resistor sensitive mask, a desired NiCr film profile is normally requested due to layout design. Figure 4(b) shows desired reference uniformity profile was obtained through this fine tuning approach. This fine-tuning approach is a novel and advanced technique to achieve best device performance and highly stable electrical properties.

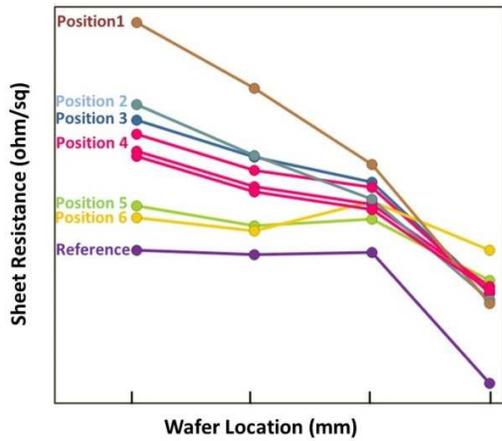


(a) Die sort map and resistor value distribution with sputter shield design A

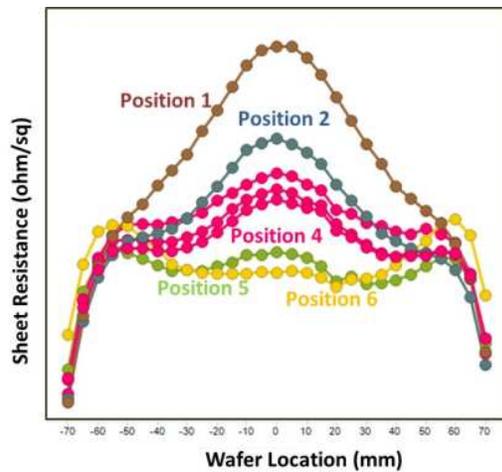


(b) Die sort map and resistor value distribution with sputter shield design B

Figure 3. Sputter shield effect on resistor value and die yield.



(a) NiCr Sheet Resistance vs. wafer location



(b) NiCr Sheet Resistance vs. and wafer locations.

Figure 4. Sheet resistance of NiCr film at different location of a wafer for different wafer position.

NiCr Thin Film Resistor Defect Reduction

NiCr particles can be introduced during sputter deposition, especially at the beginning of a target life. Figure 5 shows particle counts at different target life. Particle counts decreased sharply at very beginning of target life. In the mean time, a trend of sheet resistance measurements was also observed that indicates unstable deposition rate or film properties at the beginning of target life. Therefore a target burn-in procedure was developed using high power process to reach a stable NiCr deposition and low particle formation.

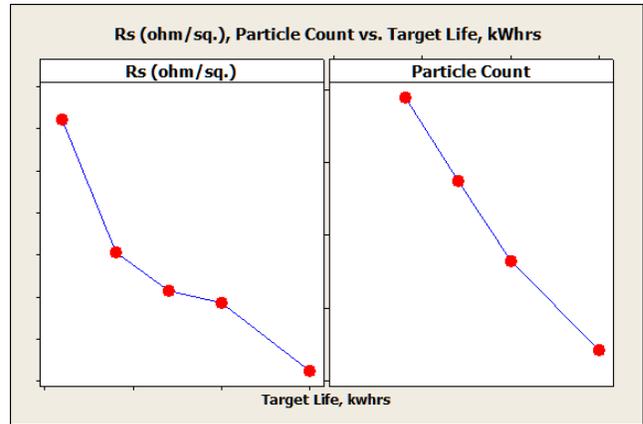


Figure 5. Sheet resistance and particle count for NiCr sputter deposition at the beginning of target life.

After NiCr liftoff process post sputter deposition, a halo defect was found around NiCr feature, as shown in Figure 6. EDS analysis indicated this type of defect was caused by carbon residue. Another set of rinse and

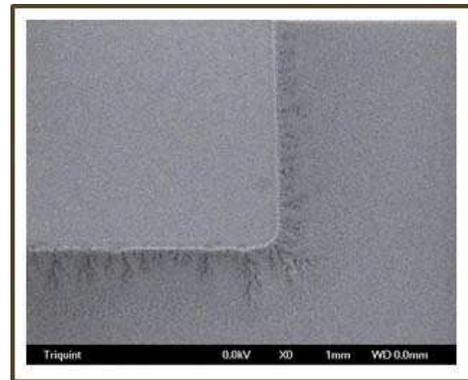


Figure 6. SEM Image of NiCr halo defect.

dry procedure could remove this type of residue. This defect was determined to have strong correlation with dryer PM schedule. Therefore a dryer clean recipe was developed to remove carbon residue source in dry process. The clean recipe is running on a regular schedule to eliminate this type of defect on NiCr resistor.

Another type of defect found on NiCr resistors, called white “particles” were formed after NiCr passivation (Figure 7). STEM images showed this defect was due to nitride delamination from NiCr features. To eliminate this defect, an ash process was implemented to remove any organic residue on the top of NiCr resistor features.

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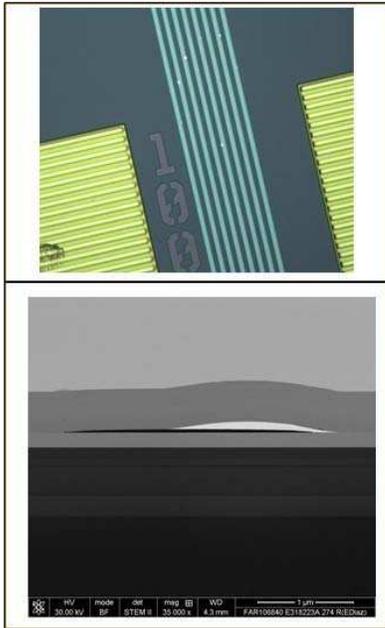


Figure 7. Optical and STEM Images of NiCr white “particles”.

Black particles were found grown on NiCr resistors after liftoff but before passivation. As shown in Figure 8, those particles had high Cr and oxygen content using EDS and Auger analysis. This type of defect was found to be related to the staging time between NiCr film liftoff and passivation. About 40% wafers staged for long time between NiCr liftoff and passivation have such defect. For all the lots staged shorter time, no black particles were observed. Therefore we implemented a queue time limit at these steps to prevent Cr oxide formation.

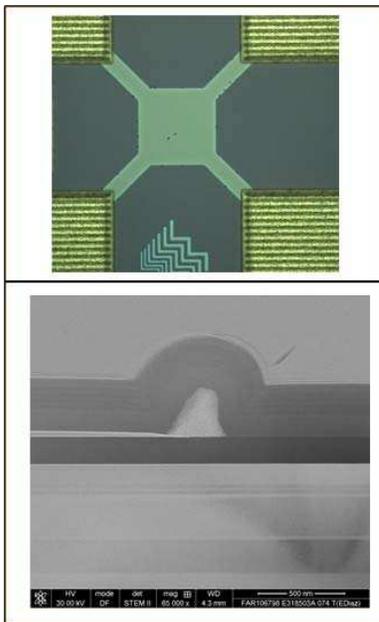


Figure 8. Optical and SEM Images of NiCr black particles.

CONCLUSIONS

We have demonstrated an optimized NiCr process in a high volume production GaAs fabrication line. Process parameters, shield design were optimized to achieve best within-wafer uniformity. A novel fine-tune approach is introduced for NiCr resistor sensitive masks. Different types of defects formed during sputter, liftoff and passivation process were identified and eliminated to ensure NiCr resistor high stability.

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ACRONYMS

TCR: Temperature Coefficient of Resistivity

NiCr: Nickel-Chromium