

Reduction in Current Leakage Fails Through an Improved Metal Lift-off Process

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Abstract

The manufacture of heterojunction bipolar transistors (HBT) may involve the use of metal lift-off (MLO) processes used to pattern the devices. Such MLO processes have been known to cause surface damage to devices. This surface damage has been attributed to reduced electrical performance, specifically, an increase in capacitor current leakage. A method has been developed that reduces device damage and current leakage fails.

INTRODUCTION

One method to achieve a patterned array of metal layers on a wafer is through the use of a MLO process. Once the wafer is resist patterned, such that the areas where metal is not wanted contain a resist, the metal layers may be deposited over the surface. MLO involves chemical and/or mechanical removal of the resist/metal stacked layers thereby leaving metal on the surface in areas that were not covered in resist.

Product and process design play important roles in minimizing MLO defects such as residual metal along feature sidewalls, and damage to devices as the metal being removed comes in contact with metal that remains. Design factors that allow for easy chemical incursion to the resist improve the likelihood of a damage-free MLO process. Such factors can include not bridging metal to unwanted metal during deposition, the use of a highly soluble lift-off resist (LOR) under the resist to receive the metal deposit, not pinning metal to the substrate on the outer wafer edge, allowing sufficient open area for the lift-off chemical to access through proper device layout and adequate resist thickness, lifting metal from a single instead of multi-level surfaces at the same time, minimizing resist hardening, and others.

A method has been developed to minimize device damage during the lift-off process itself when not all optimal design factors can be implemented.

DEFECT ANALYSIS

Microscope inspection in dark-field view post MLO revealed the presence of fine scratches across devices as shown in Figure 1. These defects were not observed prior to MLO, such as after mask and after metal deposition. A cross-section of a similar scratch was obtained and is shown in Figure 2.

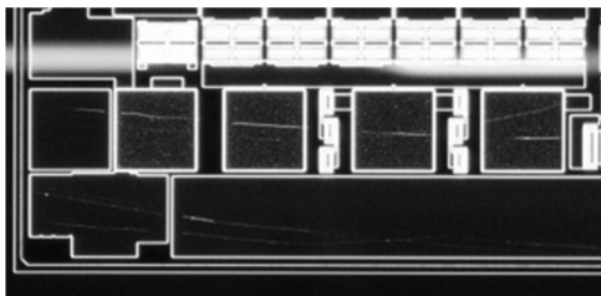


Figure 1: Fine surface scratches across capacitors post MLO.

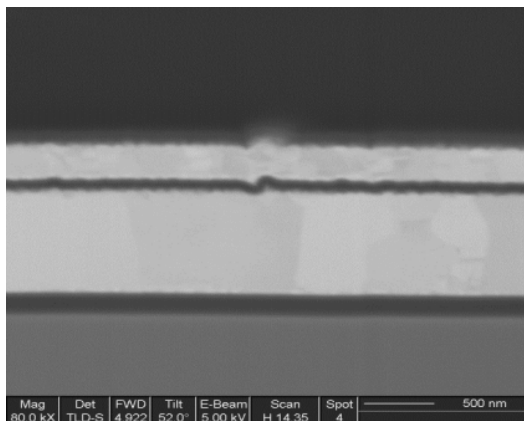


Figure 2: Cross-section of a surface scratch.

Bright-field optical microscopy revealed on-mesa metal damage post MLO as shown in Figure 3. Such damage also was not observed after mask or after metal deposition. An automated visual inspection (AVI) technique detects these defects, which are described as Pattern Bright defects.



Figure 3: On-mesa metal damage caused by MLO process, described as Pattern Bright defects.

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DEFECT REDUCTION EXPERIMENTS

Typically a multi-step MLO process is performed combining soak, spray, and rinse/dry. Process variables were changed in an effort to reduce the described defects. The soak step variables changed were time, temperature, and agitation rate during conditioning in hot solvent. Spray variables changed were spray time, spray pressure, spray arm scan speed, spray nozzle angle, wafer spin speed, and additive hot solvent during the heated solvent spray process. Wafers from a common lot were split between existing process of record (POR) recipe and experimental recipes. Wafers were processed then inspected by microscope and AVI methods.

To determine the effect of processing on the scratch rate a wafer was placed under the microscope in dark-field view and each die in two rows across the full wafer width was examined for scratches. Approximately 200 dice were examined per wafer. The number of dice with at least 1 scratch was then tabulated. Size and number of scratches on each die were not factored, so a die with multiple deep scratches and a die with a single small scratch each counted the same – 1 die scratched.

Every die on each wafer was then examined for Pattern Bright defects using AVI. The scratches visible in dark-field microscopy are not visible to the AVI. It has been determined from previous studies that the major MLO defect at AVI is Pattern Bright defects; however, any such defect that was determined to be due to a scratch from a wafer wand, for example, was excluded from the analysis.

Beyond reliability concerns the effect of MLO defects on device performance was unknown. Current leakage was a suspected result given the potential for the scratches to thin the underlying dielectric material. Tests were performed by measuring current leakage at three voltage stress conditions, low, medium and high. After the high voltage measurement cap leakage was again measured at the low voltage condition.

Once process variables were found that reduced surface defects multiple lots and circuits were split between POR and the new recipe. A total of 6 lots were analyzed for scratches using dark-field microscopy. All lots were measured for Pattern Bright defects in the AVI immediately after MLO. The first 3 lots (lots 1-3) that went on to get current leakage testing were tested at AVI using the existing AVI recipe for that particular circuit. The next 3 lots (lots 4-6) were tested at AVI using an enhanced recipe to better detect Pattern Bright defects. Current leakage for lots 4-6 has yet to be completed.

RESULTS

It was found that the wafer spin speed and the amount of solvent on the wafer during the MLO spray process affected the number of scratches and Pattern Bright defects [1]. Figures 4-9 show the reduction in scratches observed with preferred MLO recipes for lots 1-6. Normalized DF scratches were determined by dividing the number of dice scratched by the mean of scratches for all POR wafers. In the figures

below “Spin” refers to changing the wafer spin speed. “Spin+Fluid” refers to dosing the wafer surface with extra solvent during the adjusted spin spray process. Some lots received only an adjustment in wafer spin speed, some an adjustment in spin speed and surface fluid, and some lots received both.

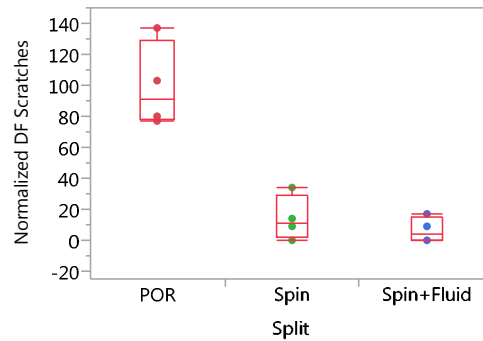


Figure 4: Lot 1, circuit A. Effect of MLO process variable on dark-field visible scratches.

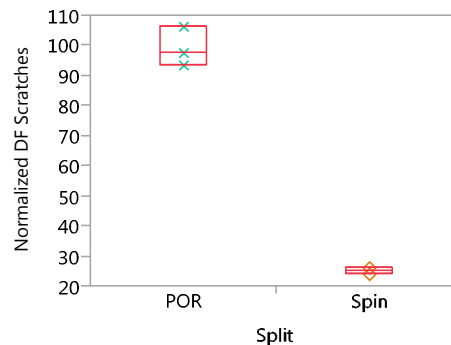


Figure 5: Lot 2, circuit A. Effect of MLO process variable on dark-field visible scratches.

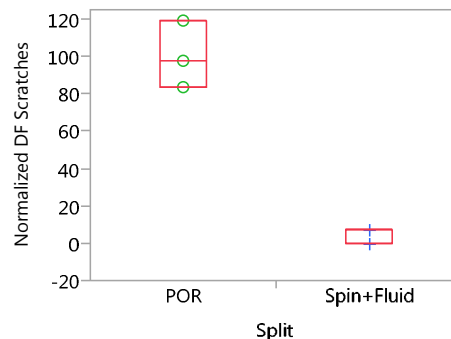


Figure 6: Lot 3, circuit B. Effect of MLO process variable on dark-field visible scratches.

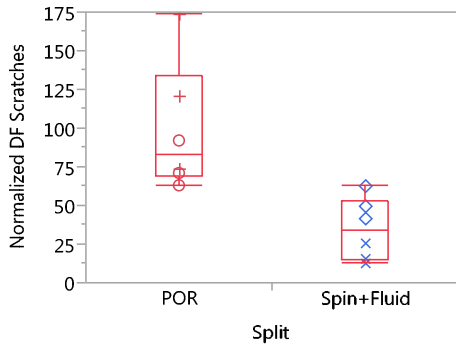


Figure 7: Lot 4, circuit C. Effect of MLO process variable on dark-field visible scratches.

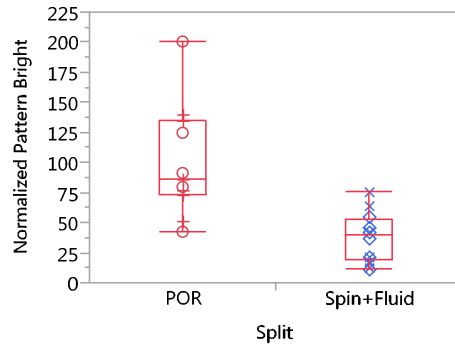


Figure 10: Lot 4, circuit C. Effect of MLO process variable on AVI Pattern Bright defects.

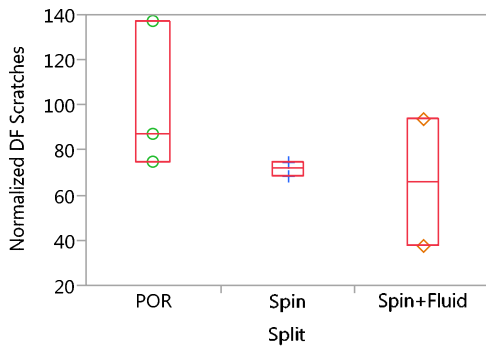


Figure 8: Lot 5, circuit D. Effect of MLO process variable on dark-field visible scratches.

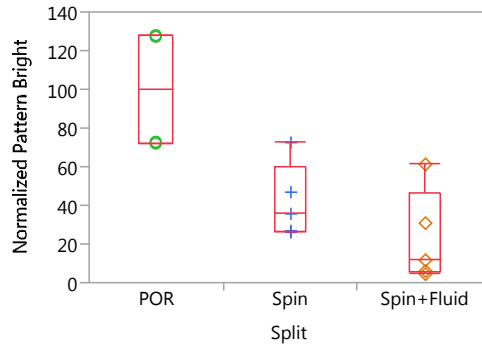


Figure 11: Lot 5, circuit D. Effect of MLO process variable on AVI Pattern Bright defects.

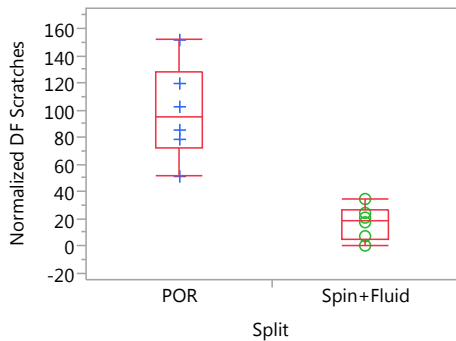


Figure 9: Lot 6, circuit D. Effect of MLO process variable on dark-field visible scratches.

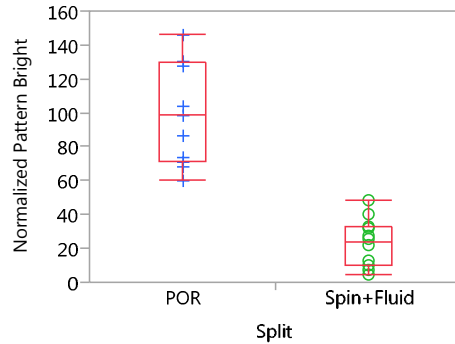


Figure 12: Lot 6, circuit D. Effect of MLO process variable on AVI Pattern Bright defects.

Figures 10-12 demonstrate the effect of MLO processing on Pattern Bright defects using an AVI recipe that enhanced such defects. Normalized Pattern Bright defects were determined by dividing the number of defects for each wafer by the mean of the Pattern Bright defects for all POR wafers.

Figure 13 shows the current leakage results in terms of normalized defect density for lots 1-3. The defect density (DD) was obtained by counting the number of fails at the medium stress test and dividing by the total capacitor test area. The DD for the split lots was then obtained by normalizing to the mean and median of the POR defect density. "F2" refers to the medium voltage stress test. A fail at F2 corresponded to leakage current greater than 100 nA. Dice containing any AVI defect were removed from the analysis in order to better correlate current leakage fails to fine scratches caused by MLO, yet not visible to the AVI.

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This does have the consequence of also removing dice with Pattern Bright defects caused by the MLO process from the analysis.

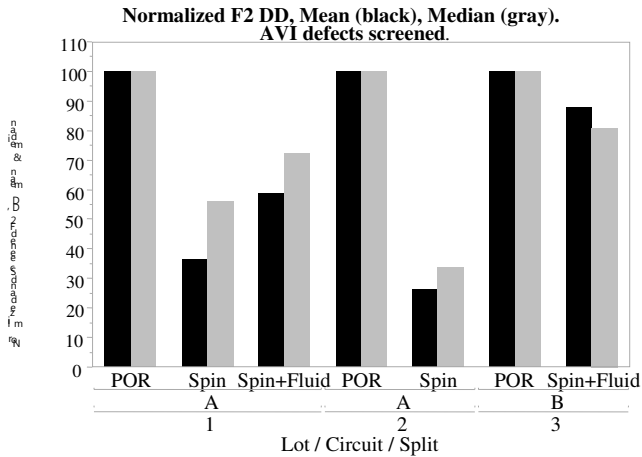


Figure 13: Current leakage fails as a function of MLO process.

There is a direct relationship between fine scratches, on-mesa metal feature damage and current leakage. However, the circuit layout is an important consideration. For example, the reduction in current leakage fails for lot 3 was less than that of lots 1 and 2 because there was much less capacitor area for circuit B compared to circuit A. This may have been predicted by the count of fine scratches if only the scratches across capacitors, not other devices on the dice were tabulated.

CONCLUSION

When the resist under the metal cannot be softened enough within an allowable time the metal surface features can be damaged during the high pressure spray step needed to remove the unwanted metal. The suggested mechanism for the defect reduction is that the impact force of lifted metal debris sliding over device features is reduced by adjusting the wafer spin speed. Supplying additional fluid to the surface during the spray process can further reduce defects by encapsulating the lifted metal as it slides across the wafer surface during removal, thus better protecting the device features from gouging.

Such MLO process conditions were shown to greatly decrease fine scratches and on-mesa metal feature damage. Not only the amount of defects, but also the severity of the defects was reduced, which the analysis methods used could not readily identify. Further work collecting cross-section

images is needed. In addition, the reduced defects were shown to drive down current leakage on capacitors.

ACKNOWLEDGEMENTS

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REFERENCES

- [1] C. Carpenter, *Optimization of a Metal Liftoff Process in a GaAs Semiconductor Device*, 2005 GaAs MANTECH Technical Digest, 2005.

ACRONYMS

- HBT: Heterojunction Bipolar Transistor
- MLO: Metal Liftoff
- LOR: Liftoff Resist
- AVI: Automated Visual Inspection
- POR: Process of Record
- DD: Defect Density