Recovery in dc Performance of Off-State Step-Stressed AlGaN/GaN High Electron Mobility Transistor with Thermal Annealing

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Abstract

   The effects of thermal annealing on dc performance of off-state drain-voltage step-stressed AlGaN/GaN high electron mobility transistors were investigated. Degradations of increasing reverse-biased gate leakage current and sub-threshold swing, as well as reducing saturating drain current and drain current on-off ratio were observed after reaching a critical voltage during the step-stressing. Interestingly, the degradations of dc performance for the stressed HEMT were recovered after a thermal annealing at 450 °C for 10 mins. HEMT integrated with an on-chip trapezoid-shape heater was proposed to realize a self-healing device.

INTRODUCTION

   AlGaN/GaN-based high electron mobility transistors (HEMTs) are outstanding candidates for high power and high frequency applications [1,2]. However, growth or process induced traps affect the breakdown voltage, gate leakage current and current collapse [3-5]. These issues impede the advancement of GaN-based power and high frequency device technology. Thermal annealing at around 400 – 450 °C are commonly used to remove dry-etching damage after plasma based gate recess etching process for AlGaN/GaN HEMTs to reduce gate leakage current and restore the Schottky gate contact. Post-process annealing was also reported to be effectively reducing gate leakage current and increasing gate breakdown voltage in AlGaN/GaN HEMTs [6,8].

   In this work, the effects of thermal annealing on off-state drain voltage step-stressed HEMTs were investigated. Saturation drain current, sub-threshold drain leakage current, sub-threshold swing, forward and reverse bias gate I-V characteristics of the stressed and annealed HEMTs were used to determine the degree of device degradation after electrical stress and the recovery after thermal annealing. A self-healing device design was proposed by integrating an on-chip heater with the HEMT. Further, finite element based 3D thermal simulations were implemented to study the temperature uniformity of the HEMT during the operation of the on-chip heater.

EXPERIMENT

   The HEMT device structures were grown on semi-insulating 6H-SiC substrates, and consisted of a thin AlN nucleation layer, 2.25 μm of Fe-doped GaN buffer, 15 nm of $Al_{0.28}Ga_{0.72}N$, and a 3 nm undoped GaN cap. On-wafer Hall measurements showed a sheet carrier concentration and mobility of 1.06×10^{13} cm^{-2} and 1907 cm^2/V-s, respectively. Device isolation of Double-finger HEMTs was achieved with dry-etch based mesa definition. Ti/Al/Ni/Au Ohmic contacts were alloyed at 850 °C, producing a contact resistance of 0.3 Ω-mm. Dual-finger Ni/Au gates were defined by standard lift-off and the gate dimension was 2×1 μm $\times$ 150 μm. Schottky barrier height of Ni/Au gates was around 0.8 V. The HEMTs were passivated with 120 nm SiN$_x$ deposited by plasma enhanced chemical vapor deposition.

   Off-state drain-voltage step-stress was employed to degrade the dc performance of the HEMTs. The stress started at 5 V of drain voltage, while grounding the source electrode and fixing the gate voltage at -8 V. The increment of the drain voltage step was 1 V, and each drain voltage step was pulsed constantly for 1 minute until a critical voltage was reached. The critical voltage was defined as the onset of a sudden total gate leakage current increase during the stress. Thermal annealing effect was conducted for the post-stress HEMTs at 450 °C for 10 mins in nitrogen ambient using a SSI Solaris 150 rapid thermal annealing (RTA) system.

DISCUSSION

   The critical voltages of HEMTs employed in this study were around 30-50 V. After HEMT reaching the critical voltage during the off-state step-stressing, dc performance of the stressed HEMT considerably degraded. Increases of sub-threshold swing and sub-threshold leakage current, as well

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as reductions of saturation drain current and drain current on-off ratio were observed as shown in Figure 1. Due to the low drain-to-source current during off-state stressing, self-heating effects were negligible and had no effect on the device degradation. A notch usually appeared on drain side or on both drain and source sides of the gate finger for the degraded HEMT after step-stressing due to the inverse piezoelectric effect [9]. There are regions exhibiting interactions between Ni of the Au/Ni based Schottky gate with the underlying nitride layer close to a position of threading dislocation (TD) [9]. The interaction of Ni and underlying nitride layer was also observed on the thermally annealed HEMTs [9]. The notch formation around the edges of gate fingers and the interaction between Ni and nitride layer resulted in increasing sub-threshold swing and sub-threshold leakage current, as well as decreasing saturation drain current and drain current on-off ratio.
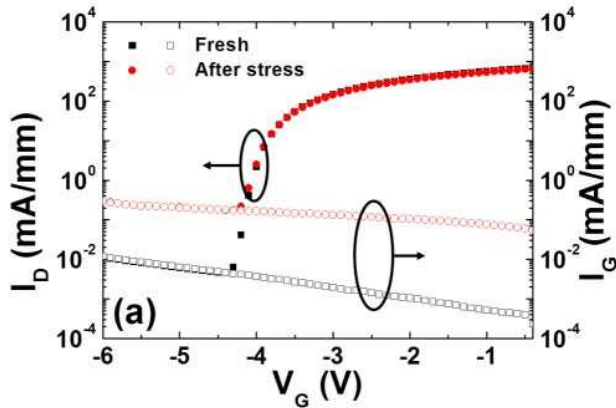

Figure 2. Gate voltage dependent drain current and gate leakage current of AlGaN/GaN HEMTs after second step-stressing and after second thermal annealing.

Drain current sub-threshold swing was employed to investigate the number of trap densities created in HMETs after off-state step-stressing [10,11]. Drain current sub-threshold swing has been commonly used to estimate trap densities in metal oxide semiconductor field effect transistors and AlGaN/GaN HEMTs. The sub-threshold swing increased from ~98 to ~187 mV/dec after step-stressing and recovered back to ~95 mV/dec after thermal annealing. Temperature dependent sub-threshold swings were measured to determine the corresponding interface trap density of HEMTs at different stages of this study. The trap density of the reference HEMT was around 2.15×10^{12} /cm^2-V. After the first and the second step-stressing, the trap density increased to 6.31×10^{12} and 6.19×10^{12} /cm^2-V, respectively. The trap density recovered to 3.56×10^{12} and 4.81×10^{12}/cm^2-V after the first and second thermal annealing, respectively. It is possible that the neutral traps are charged during the device operation from the hot electrons. These negative charges on the HEMT surface and in AlGaN as well as GaN channel layer would alter the conduct band bending, reduce the carrier concentration in the two dimensional electron gas channel and increase the gate leakage current. The thermal annealing could provide energy for charged traps to go through a de-trapping process and become neutral traps.

Figure 1. Gate voltage dependent drain current and gate leakage current of AlGaN/GaN HEMTs prior to and after off-state step-stressing.

Interestingly, as shown in Figure 2, previously described degradations of HMET dc performance resulted from off-state step-stressing after reaching the critical voltage were completely recovered with a thermal annealing at 450 °C for ten minutes. Similar dc degradations were observed for those annealing recovered HEMTs after second off-state drain-voltage step-stressing, and the dc performance of the degraded HEMTs was fully recovered again after a second 450 °C thermal annealing. This indicated that defects created during the off-state step-stressing could be recovered by a thermal annealing. Apparently, the thermal annealing process could not remove this metal diffusion nor the notch formation along the gate edges. Thus, gate metal diffusion and notch formation on the AlGaN/GaN layer after off-state step stress or thermal annealing were not related to the degradations of the dc performance. These degradations could result from creating shallow traps during off-state step-stressing, and these traps were able to be annealed out with the thermal annealing process.
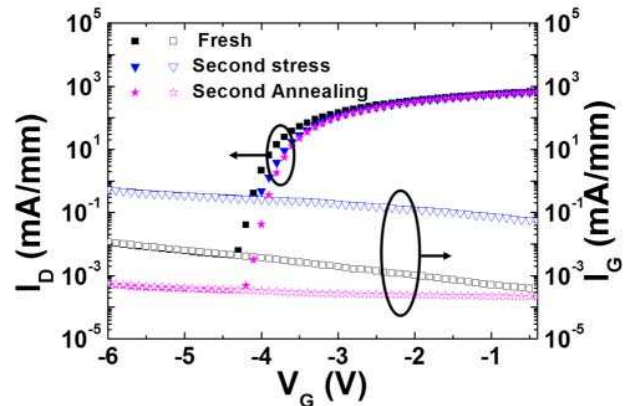
Although the thermal annealing in the RTA system could recover the device degradation, this process would be able to be applied to the HEMTs in the packaged integrated circuit or system. A shown in Figure 3, an on-chip heater was designed to accomplish the same annealing process for the discrete HEMTs. Pt-based heater was employed as the heating element. A trapezoid configuration was proposed for the heater to achieve uniform temperature distributions across the active region by reducing the resistance in the middle section of the heater. The Pt-based heater extended over the gap between source and gate, and extended 1.5 μm over the gate edge toward the drain.

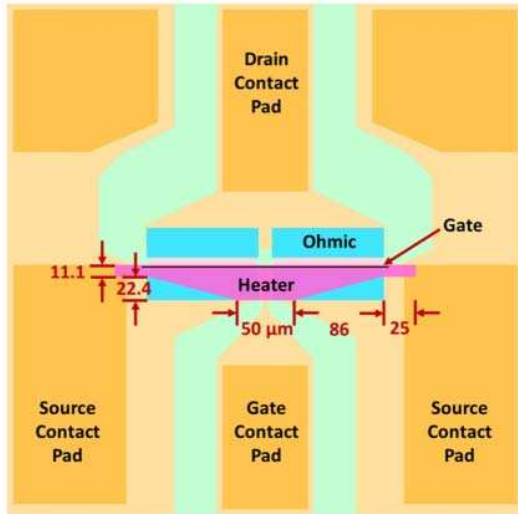CS ManTech Conference, May 16th - 19th, 2016, Miami, Florida, USA

Figure 3. Schematic of HEMT integrated with an on-chip heater.

The junction temperature of the HEMT integrated with an on-chip heater can be increased by applying a bias voltage across the source contact pads. By applying 19 V across a 300 nm Pt heater, a maximum temperature of 467 °C was reached under the gate region, as shown in Figure 4. Similar design has been made for the multiple-finger power transistor. The thermal simulation result for the multiple-finger transistor will be presented in the meeting.
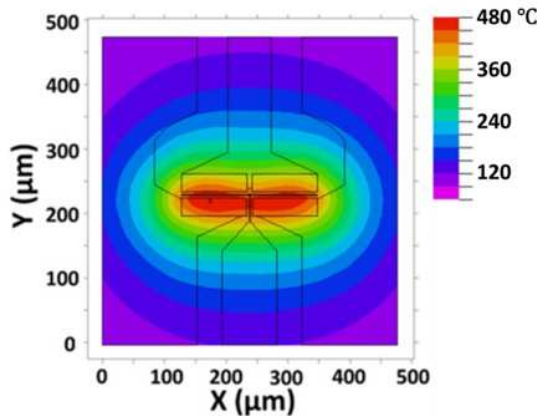

Figure 4. Thermal simulated junction temperature of a HEMT with an integrated trapezoid shape heater.

CONCLUSIONS

The effects of thermal annealing on dc performance of off-state step-stressed HEMT were investigated. Device degradations of drain current reduction and increases of parasitic resistance and gate leakage current were completely recuperated after annealing at 450 °C for 10 minutes. HEMT integrated with an on-chip trapezoid-shape heater was proposed to realize a self-healing device.

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ACRONYMS

HEMT: High electron mobility transistor
RTA: Rapid thermal annealing
TD: Threading dislocation
TEM: Transmission electron microscopy

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