

Reliability Assessment of Thermally-Stable Gate Materials for AlGaIn/GaN HEMTs

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Keywords: GaN, HEMT, Reliability, TiN, Nanocrystalline Diamond

Abstract

TiN and nanocrystalline diamond have been evaluated as potential replacements for conventional Ni-based gate schemes in AlGaIn/GaN HEMTs using reverse bias electrical stressing. TiN gates deposited by atomic layer deposition were found to be viable substitutes, as TiN-gated devices exhibited improved on-state characteristics in comparison to the Ni/Au-gated devices. TiN was also determined to have a much higher critical reverse gate voltage ($V_{gs} = -210$ V for TiN vs. -120 V for Ni/Au) at which gate degradation occurs. The TiN gates also catastrophically failed at slightly higher and much less variable breakdown voltages than the Ni/Au gates. Stressing at reverse gate biases slightly above the Ni/Au critical voltage but well below the TiN critical voltage ($V_{gs} = -140$ V) led to nearly an order of magnitude increase in leakage current for the Ni/Au, but decreased leakage in the TiN. Nanocrystalline diamond gates exhibited critical voltages of $V_{gs} = -90$ V and broke down at much lower reverse bias, possibly due to testing in air without encapsulation to protect the gate material.

INTRODUCTION

AlGaIn/GaN high electron mobility transistors (HEMTs) commonly rely on Ni/Au-based Schottky gate metallizations that have been shown to degrade when subjected to electrical stress, thermal stress, and radiation due to Ni migration into adjacent metal or semiconductor layers.[1–5] The instability of these Ni-based gates limits device reliability, rendering the search for alternative gate materials that are electrically and thermally stable a topic of tremendous importance. Materials such as the transition metal nitrides (TiN, etc.) and boron-doped nanocrystalline diamond represent candidate materials for replacement of the Ni-based gates. Of the transition metal nitrides, TiN is a particularly promising material, due to its near-metallic conductivity, suitable Schottky barrier heights and ideality factors on GaN and AlGaIn, and high temperature stability.[6–8] These nitrides can be easily deposited by atomic layer deposition (ALD), sputtering, or molecular beam epitaxy (MBE), which is particularly attractive due to the ability to deposit *in-situ* immediately after the AlGaIn/GaN growth without exposing

the material to atmosphere, thereby further improving device quality and reliability. Boron-doped p⁺ diamond gates have also been shown to be candidates for HEMT gates and are attractive due to the high thermal conductivity and low leakage in the heterojunction gate.[9,10]

Though these materials show promise for HEMT gates, little work has been done to assess their contributions to device reliability under extended electrical or thermal stress.[8,11] In this work, the reliability of TiN and p⁺ nanocrystalline diamond (NCD) as gate materials for AlGaIn/GaN HEMTs is evaluated through the use of reverse bias electrical stressing.

EXPERIMENTAL

Devices with Ni/Au, TiN, and p⁺ diamond gates (shown schematically in Figure 1) were fabricated from an AlGaIn/GaN HEMT structure grown by metal organic chemical vapor deposition (MOCVD) on a SiC substrate, consisting of an AlN nucleation layer, Fe-doped GaN buffer, AlN interlayer, and an undoped Al_{0.22}Ga_{0.78}N barrier layer.[12] Hall effect measurements indicated that the two-dimensional electron gas (2DEG) carrier density and mobility were 9.4×10^{12} cm⁻² and 2070 cm²/(V·sec), respectively. The devices had a gate-source spacing of 2 μm, a gate length of 3 μm, gate-drain spacing of 10 μm, and gate width of 75 μm. Device mesas were fabricated using Cl₂-based inductively coupled plasma (ICP) etching. Ohmic contacts were formed by lift-off and rapid thermal annealing (RTA) of electron-beam (e-beam) evaporated Ti/Al/Ni/Au metal. After Ohmic contact processing, all devices were passivated with 100 nm plasma-enhanced chemical vapor deposition (PECVD) SiN_x. SF₆-based reactive ion etching (RIE) was used to open gate and overlay windows in the SiN_x. On the reference sample, Ni/Au gates were fabricated by e-beam evaporation and lift-off. TiN-gated HEMTs were fabricated by atomic layer deposition (ALD) of 75 nm TiN, followed by e-beam deposition and lift-off of Ti/Au contacts. The Ti/Au was then used as an etch mask for self-aligned SF₆-RIE etching to remove the TiN outside the device gate regions. NCD gates were fabricated by blanket growth of 500 nm boron-doped nanocrystalline diamond by microwave chemical vapor

deposition (MW-CVD).[13] After NCD growth, Ti/Al/Ni/Au gate contacts were fabricated by e-beam deposition and lift-off; the contacts were then used as a self-aligned etch mask for removal of NCD outside the gate regions using an O₂-RIE etch.[14] Overlay metal was deposited on all samples by lift-off of e-beam evaporated Ti/Au.

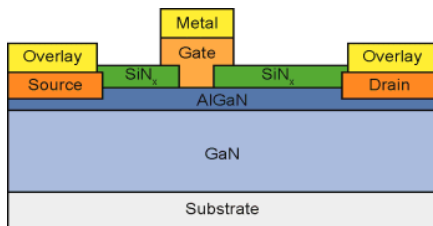


Figure 1. Schematic of the HEMT devices fabricated in this study. (The gate/metal stack consisted of Ni/Au, TiN/Ti/Au, or NCD/Ti/Al/Ni/Au.)

RESULTS AND DISCUSSION

Device Performance

As-fabricated device performance was evaluated via static I-V measurements using a Keithley 4200 Semiconductor Characterization System; relevant parameters for each device listed in Table I and shown graphically in Figures 2 and 3. The TiN-gated HEMTs offered improved on-state characteristics in the form of higher maximum transconductance ($g_{m,max}$), higher maximum on-state drain current ($I_{ds,max}$), and lower on-resistance (R_{on}) than the Ni/Au-gated HEMTs, albeit at the expense of higher off-state gate and device leakage (I_{off}). Hall Effect measurements were also performed on gated van der Pauw patterns fabricated with the devices to characterize the effects of the recess etch and gate deposition processes on the 2DEG density (n_s) and carrier mobility (μ_{2DEG}). The decreased 2DEG density and mobility of the Ni/Au devices relative to the as-grown structure was attributed to fluorination of the AlGaIn barrier layer during the recess etch. The TiN-gated devices were less degraded, as the structure was effectively annealed during the TiN growth process (350 °C for multiple hours).[15] The on-state performance and Hall characteristics of the NCD-gated HEMTs was worse than expected in comparison to previous results; this could be due to either nonuniform boron doping or damage to the AlGaIn barrier during diamond growth.[9]

TABLE I
DEVICE PARAMETERS FOR Ni/AU-, TiN-, AND NCD GATED HEMTs

Parameter	Units	Gate Material		
		Ni/Au	TiN	NCD
V_t	V	-2.47	-2.77	-2.98
I_{off} ($V_{gs} = -10V$)	mA/mm	0.179	4.88	0.448
$g_{m,max}$	mS/mm	140	159	101
$I_{ds,max}$ ($V_{gs} = 1V$)	mA/mm	491	589	413
R_{on}	Ω -mm	8.61	8.10	18.1
n_s	cm ⁻²	6.76×10^{12}	7.75×10^{12}	$< 1 \times 10^{12}$
μ_{2DEG}	cm ² /(V·sec)	1890	1950	n/a

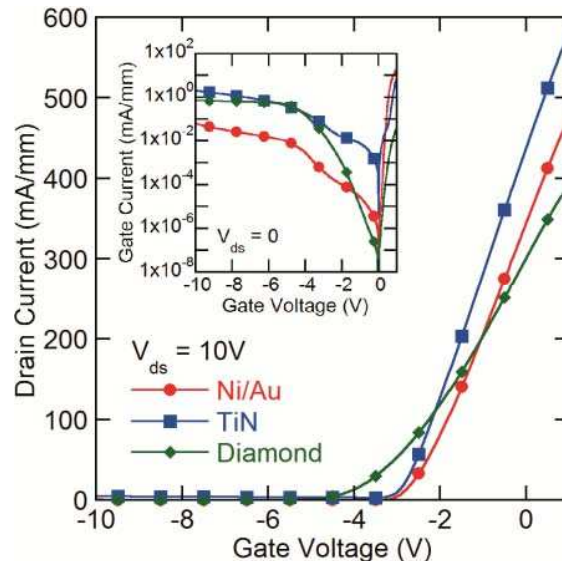


Figure 2. Turn-on (I_{ds} - V_{gs}) characteristics at $V_{ds} = 10V$ for HEMT devices with Ni/Au, TiN, and NCD gates; inset shows gate current as a function of gate voltage for $V_{ds} = 0V$.

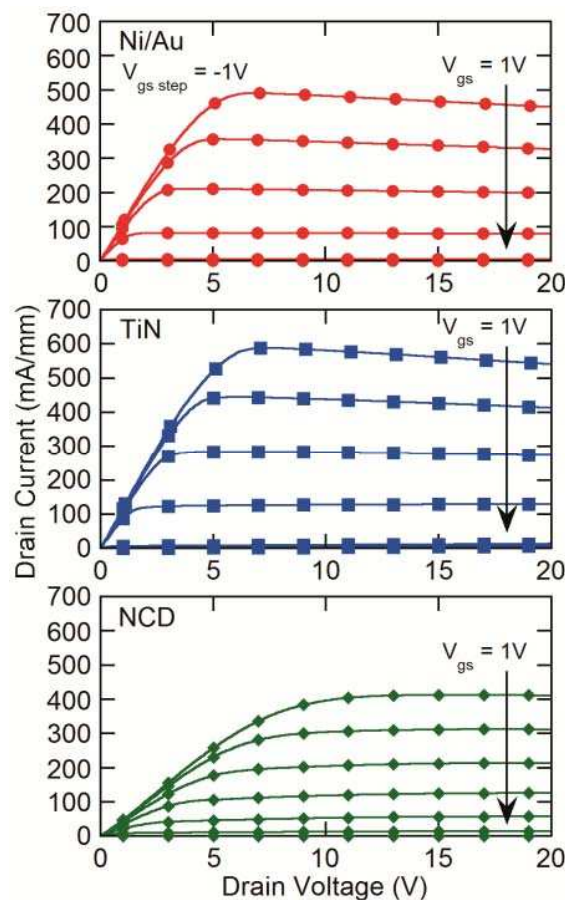


Figure 3. Static drain current-drain voltage (I_{ds} - V_{ds}) behavior for Ni/Au, TiN, and NCD-gated HEMTs. (V_{gs} ranged from -10 V to 1 V in 1 V steps.)

Electrical Stressing

All three device schemes were initially tested by reverse bias sweeping from $V_{gs} = 0$ to breakdown, as shown in Figure 4. The Ni/Au-gated HEMTs exhibited a critical voltage of $V_{gs} = -120$ V, as evidenced by the sudden increase and subsequent instability in gate leakage for higher reverse voltage; this is consistent with previous reports of Ni/Au gate instability under reverse bias stressing.[16] TiN gates were found to exhibit a much higher critical voltage of $V_{gs} = -210$ V, albeit with significantly higher overall leakage in comparison to the Ni/Au. This may stem from the lower barrier height at the TiN/AlGaIn interface, owing to the lower (and variable) work function of TiN in comparison to Ni/Au, or from the formation of a leaky surface layer at the interface during the initial stages of TiN growth.[7,8,17–19] The NCD-gated HEMT exhibited stable gate current to only $V_{gs} = -90$ V; beyond this voltage, the device gate current steadily increased until the gate failed catastrophically at only -160 V. These devices failed as an open gate rather than a short in the case of the previous two devices. It is possible that the gate may have been etched by the ambient atmosphere due to self-heating during reverse bias stressing.[20] As this failure mechanism is poorly understood and potentially unstable, NCD gate devices were excluded from subsequent stress experiments. Further testing in vacuum and/or encapsulation of the device will be employed to probe this failure mode in more detail.

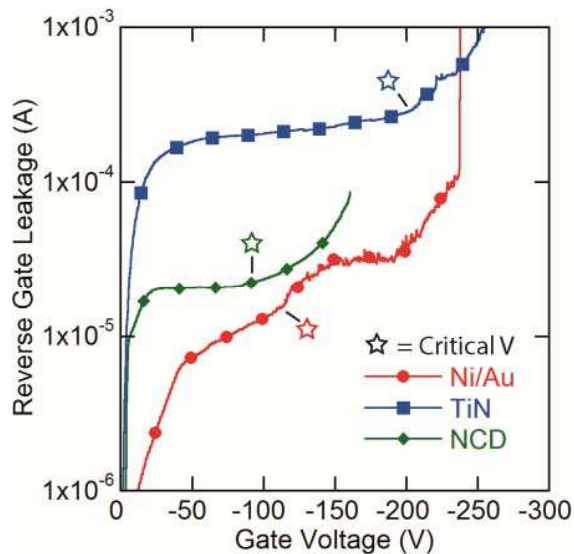


Figure 4. Gate leakage during gate voltage sweeping from 0V to reverse breakdown for Ni/Au-, TiN-, and NCD-gated HEMTs. Critical voltage limits after which gate degradation occurs are marked for each gate scheme.

To further assess the breakdown characteristics of the Ni/Au and TiN gates, five HEMTs with each gate scheme were tested to breakdown under step-stress measurements, as shown in Table II. The Ni/Au gates failed catastrophically at varying reverse bias, ranging from -210 V to -270 V, with an average breakdown voltage of approximately -240 V. The TiN failed at a much narrower

voltage range (around -270 V), indicating that the TiN gates had both a slightly higher reverse breakdown voltage, as well as a more consistent range of reverse bias failure conditions.

TABLE II
BREAKDOWN VOLTAGES FOR Ni/AU- AND TiN- GATED HEMTs

Gate	Reverse Breakdown Voltage (V)	
	Individual	Average (Nearest 10V)
Ni/Au	-220	-240 ± 30 V
	-250	
	-210	
	-260	
	-270	
TiN	-250	-270 ± 10 V
	-270	
	-270	
	-270	
	-270	

Initial assessments of the time-dependent electrical stress degradation were made by holding devices at a constant gate bias of -140 V for 1 hour ($V_{ds} = 0$). This bias was selected to evaluate the stability of each gate scheme at a condition above the critical voltage that should initiate degradation (but not failure) in the reference Ni/Au devices. Gate stability was evaluated by observing the gate current during stressing (Figure 5), along with changes in the gate I-V characteristics before and after stressing (Figure 6). During this stress, the Ni/Au gate leakage at increased by nearly 225% without device failure, indicating that the gate degraded under these conditions. TiN gate leakage actually decreased to a stable value during stressing, possibly due to a self-annealing effect in the TiN during stressing. The NCD gate failed almost immediately under these conditions; this was expected given that the stress condition was significantly beyond the critical voltage identified in Figure 4.

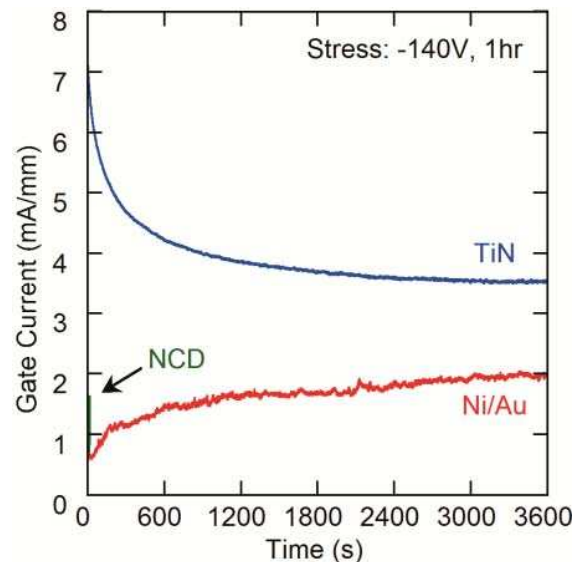


Figure 5. Ni/Au, TiN, and NCD gate during stressing at $V_{gs} = -140$ V for 1 hour. (NCD gate failed within 60 sec of stress initiation.)

10b

Comparison of the pre- and post-stress gate current confirmed that permanent degradation occurred in the Ni/Au gate after stressing above the critical voltage, as the gate leakage increased by nearly an order of magnitude after stressing. Conversely, the TiN leakage decreased as a result of the stressing, since the selected stress condition was well below the observed critical voltage for TiN. The decrease during stressing also suggests that the TiN leakage may be further reduced by annealing the gate films before testing.

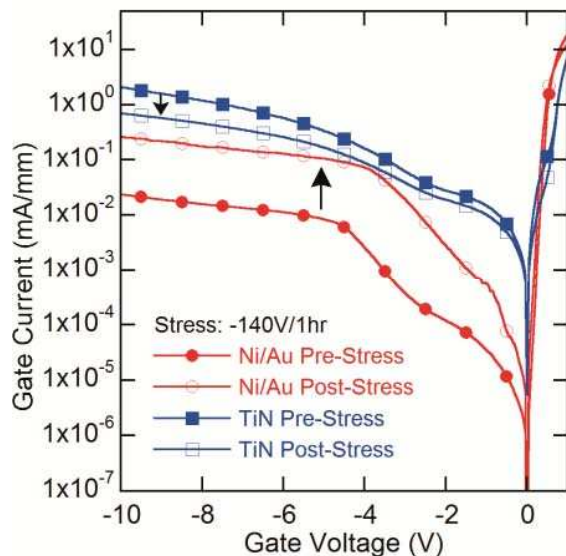


Figure 6. Ni/Au and TiN gate leakage currents before and after stressing at $V_{gs} = -140$ V for 1 hour. The Ni/Au gate leakage increased by nearly one order of magnitude after stressing, while the TiN leakage decreased.

CONCLUSIONS

Ni/Au-, TiN-, and NCD-gated HEMTs were successfully fabricated and characterized under static I-V testing. Stressing of the device gates under high reverse bias identified critical voltage conditions that led to degradation and catastrophic failure. Ni/Au gates exhibited a critical voltage around $V_{gs} = -120$ V, and failed catastrophically at voltages between -210 V to -270 V. TiN gates exhibited a significantly higher critical voltage of -210 V, along with much more consistent breakdown voltages around -270 V. NCD-gated HEMTs exhibited lower critical voltages of -90 V and breakdown voltages around -160 V, possibly due to gate degradation during high bias testing in the ambient atmosphere. Stressing at $V_{gs} = -140$ V (above the Ni/Au critical voltage) for one hour led to permanent degradation in the Ni/Au gates, as evidenced by higher leakage currents during and after stressing. The TiN gates improved as a result of this stress condition (below the TiN critical voltage), while the NCD gates failed almost immediately due to stressing well above their critical voltage. TiN gates are therefore expected to be more stable under high reverse bias conditions than the Ni/Au or unencapsulated NCD gates. Work is ongoing to assess the stability of these gate schemes during electrical testing at elevated temperatures.

ACKNOWLEDGEMENTS

The authors thank the NRL Institute for Nanoscience for equipment and processing support.

REFERENCES

- [1] J.-B. Fonder, L. Chevalier, C. Genevois, O. Latry, C. Duperrier, F. Temcamani, et al., *Microelectron. Reliab.* 52 (2012) 2205–2209.
- [2] C.Y. Chang, T. Anderson, J. Hite, L. Lu, C.-F. Lo, B.-H. Chu, et al., *J. Vac. Sci. Technol. B* 28 (2010) 1044–1047.
- [3] M. Dammann, M. Baeumler, P. Brückner, W. Bronner, S. Maroldt, H. Konstanzer, et al., *Microelectron. Reliab.* 55 (2015) 1667–1671.
- [4] Y.-H. Choi, J. Lim, Y.-S. Kim, M.-K. Han, *Mater. Res. Soc. Symp. Proc.* 1167 (2009).
- [5] A.D. Koehler, P. Specht, T.J. Anderson, B.D. Weaver, J.D. Greenlee, M.J. Tadjer, et al., *IEEE Electron Device Lett.* 35 (2014) 1194–1196.
- [6] J.-P. Ao, A. Suzuki, K. Sawada, S. Shinkai, Y. Naoi, Y. Ohno, *Vacuum.* 84 (2010) 1439–1443.
- [7] Y. Gotoh, H. Tsuji, J. Ishikawa, *J. Vac. Sci. Technol. B* 21 (2003) 1607–1611.
- [8] L. Li, A. Kishi, T. Shiraishi, Y. Jiang, Q. Wang, J.-P. Ao, *J. Vac. Sci. Technol. A* 32 (2014) 02B116.
- [9] T.J. Anderson, A.D. Koehler, K.D. Hobart, M.J. Tadjer, T.I. Feygelson, B.B. Pate, et al., *IEEE Electron Device Lett.* 34 (2013) 1382–1384.
- [10] A.D. Koehler, T.J. Anderson, K.D. Hobart, M.J. Tadjer, T.I. Feygelson, J.K. Hite, et al., *2014 Int. Conf. Compd. Semicon. Manuf. Technol.*, 2014.
- [11] Y.-C. Lin, C.-H. Chang, F.-M. Li, L.-H. Hsu, E.Y. Chang, *Appl. Phys. Express.* 6 (2013) 091003.
- [12] D.A. Gajewski, S. Sheppard, T. McNulty, J. Barner, J. Milligan, *J. Palmour, 26th Annu. JEDEC RoCS Work.*, 2011.
- [13] J.E. Butler, A. V. Sumant, *Chem. Vap. Depos.* 14 (2008) 145–160.
- [14] M.J. Tadjer, T.J. Anderson, K.D. Hobart, T.I. Feygelson, J.E. Butler, F.J. Kub, *Mater. Sci. Forum.* 645-648 (2010) 733–735.
- [15] Y. Cai, Y. Zhou, K.J. Chen, K.M. Lau, *IEEE Electron Device Lett.* 26 (2005) 435–437.
- [16] E. Zaroni, M. Meneghini, A. Chini, D. Marcon, G. Meneghesso, *IEEE Trans. Electron Devices.* 60 (2013) 3119–3131.
- [17] L.P.B. Lima, J.A. Diniz, I. Doi, J.G. Fo, *Microelectron. Eng.* 92 (2012) 86–90.
- [18] B. Ofuonye, J. Lee, M. Yan, C. Sun, J.-M. Zuo, I. Adesida, *Semicon.* 29 (2014) 095005.
- [19] M.T. Hirsch, K.J. Duxstad, E.E. Haller, *Electron. Lett.* 33 (1997) 95–96.
- [20] D.I. Shahin, T.J. Anderson, T.I. Feygelson, B.B. Pate, V.D. Wheeler, J.D. Greenlee, et al., *Diam. Relat. Mater.* 59 (2015) 116–121.