Suppression of Current Collapse in AlGaN/GaN MISHEMTs using *in-situ* SiN Gate Dielectric and PECVD SiN Passivation

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Abstract

This paper compares MOCVD *in-situ* SiN and PECVD SiN as the gate dielectric and surface passivation for AlGaN/GaN MISHEMTs. Combining the advantages of *in-situ* SiN gate dielectric and PECVD SiN passivation, an excellent on/off current ratio of ~10^9 and a steep subthreshold slope of 70 mV/dec, with suppressed current collapse have been achieved in the AlGaN/GaN MISHEMTs. The demonstrated bilayer SiN scheme is promising to boost the performance of GaN-based MISHEMTs for power switching applications.

INTRODUCTION

GaN-based high-electron-mobility transistors (HEMTs) are considered as one of the leading candidates for high-efficiency power switching applications, owing to the superior material properties of GaN. However, there remain problems in the Schottky gate HEMT structure, such as large gate leakage and severe current collapse. To address these issues, metal-insulator-semiconductor HEMT (MISHEMT) structures and surface passivation techniques have been extensively investigated. Various kinds of materials deposited by PECVD or ALD, including SiO_2 [1], SiN [2] and Al_2O_3 [3], have been employed as gate dielectrics. However, most of these gate dielectrics are deposited in an ex-situ manner, which might introduce high density interface trap states between the gate dielectric and the barrier, causing leakage reliability, and instability issues [4].

Recently, both our group and other researchers have reported the *in-situ* growth of SiN as a gate dielectric, i.e., the SiN layer is deposited immediately after the GaN HEMT structure epitaxy in the MOCVD system [5-7]. The devices exhibit extremely low leakage, attributed to the high-temperature and *in-situ* deposition method. Despite the fact that the *in-situ* SiN can act as a high-quality gate dielectric, much less attention has been paid to its standalone passivation capability in AlGaN/GaN MISHEMTs.

PECVD SiN has also been widely used as a gate dielectric and surface passivation for GaN MISHEMTs. However, the device performance usually highly depends on the treatment prior to the SiN deposition. Relatively high off-state leakage currents, which might be related to surface leakage or reverse gate leakage, are often observed for these devices [2].

This paper reports a comparative investigation of MOCVD *in-situ* SiN and PECVD SiN as gate dielectrics and surface passivation for AlGaN/GaN MISHEMTs, independently and combined. Low-leakage low-current-collapse AlGaN/GaN MISHEMTs are demonstrated by using an *in-situ* SiN gate dielectric and PECVD SiN passivation.

DEVICE FABRICATION

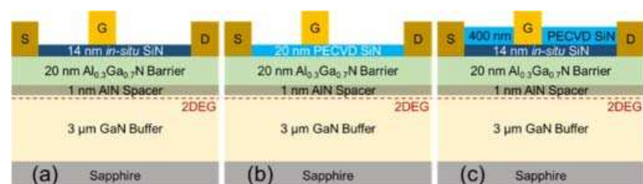

Fig. 1. Cross-sectional schematic of the MISHEMTs with (a) *in-situ* SiN only, (b) PECVD SiN only, and (c) *in-situ* SiN gate dielectric with additional PECVD SiN passivation.

In-situ SiN/AlGaN/GaN heterostructures were grown on a 2-inch sapphire substrate by MOCVD. The epilayers, from bottom to top, consist of a 3 µm unintentionally-doped GaN buffer, a 1 nm AlN spacer, a 20nm $Al_{0.3}Ga_{0.7}N$ barrier, and a 14 nm *in-situ* grown SiN cap. The SiN cap layer was grown at 1125 °C using SiH_4 and NH_3 as precursors. The device fabrication started with source/drain Ohmic contact formation using an alloyed Ti/Al/Ni/Au-based metal stack. Device isolation was performed using Ar-implantation and the gate metal was Ni/Au. Fig.1 (a) shows the cross-sectional schematic of the fabricated MISHEMTs. For comparison, a control MISHEMT sample with an identical AlGaN/GaN HEMT epi structure except the *in-situ* SiN cap, was fabricated at the same time using 20 nm PECVD SiN as a gate dielectric, (Fig.1 (b)). The PECVD SiN was deposited at 300 °C using SiH_4 and NH_3 as precursors. After the device characterization, the MISHEMTs with the *in-situ* SiN gate dielectric were passivated with an extra 400 nm of PECVD SiN (Fig.1 (c)) and characterized again.

RESULTS AND DISCUSSION

Fig.2 shows the semi-log scale plot of the transfer characteristics for the MISHEMTs with the aforementioned structures. The MISHEMTs with an *in-situ* SiN gate dielectric show a high on/off current ratio of ~ 2×10^9 and ~ 1×10^9 before and after PECVD SiN passivation, respectively, which is two orders of magnitude higher than that of the MISHEMTs with a PECVD SiN gate dielectric. The higher off-state drain leakage in the devices with the PECVD SiN gate dielectric mainly results from the reverse biased gate leakage. It can be seen that even with larger thickness, the PECVD SiN exhibits poorer leakage blocking capability, compared to the MOCVD *in-situ* SiN. This is probably due to the lower deposition temperature of the PECVD SiN, and thus worse material quality. The subthreshold slope (SS) is 68 mV/dec and 70 mV/dec for the MISHEMTs with the *in-situ* SiN gate dielectric before and after PECVD SiN passivation, respectively. Compared to that of the control sample, which is 90 mV/dec, the steeper SS suggests the superior interface quality between the *in-situ* SiN and AlGaN barrier.

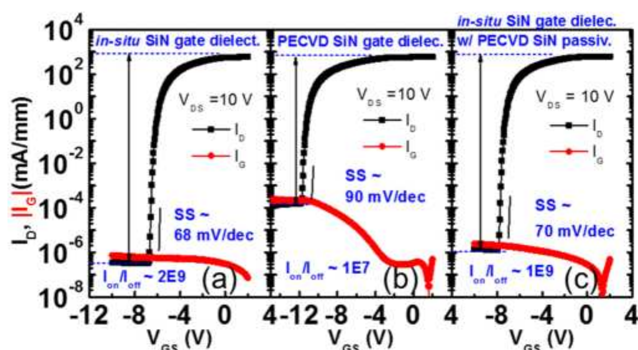

Fig. 2. Semi-log scale transfer characteristics of the MISHEMTs with (a) *in-situ* SiN only, (b) PECVD SiN only, and (c) *in-situ* SiN gate dielectric and PECVD SiN passivation. Device dimensions: $L_G/L_{GS}/L_{GD}/W_G$ = 2/3/15/20 µm.

Fig. 3 compares the passivation effectiveness of the *in-situ* SiN with PECVD SiN passivation for the AlGaN surface. Both DC and gate-pulsed IV characteristics were measured. For the pulse measurement, the quiescent bias for the gate pulse (V_{GS0}) was set at -12 V to make sure that all devices are under off-state stress. The pulse width was 500 µs and the period was 1 s. For the MISHEMTs with *in-situ* SiN gate dielectric only, severe current collapse was observed under the pulsed IV measurement, as shown in Fig.3 (a), while negligible dispersion between the DC and pulsed IV was observed for the MISHEMTs with the PECVD SiN gate dielectric (Fig.3 (b)), indicating that the passivation of the standalone *in-situ* SiN is not as effective as that of the PECVD SiN. Moreover, after the deposition of an additional 400 nm of PECVD SiN on top of the MISHEMTs with the *in-situ* SiN gate dielectric, the severe current collapse is dramatically suppressed, as shown in Fig.3 (c). These results suggest that, under a reverse gate bias, electrons injected from the gate can be trapped by deep-level trap states with long emission time constants at the *in-situ* SiN surface. The PECVD SiN passivation can eliminate such deep-level trap states, thus suppressing the current collapse.

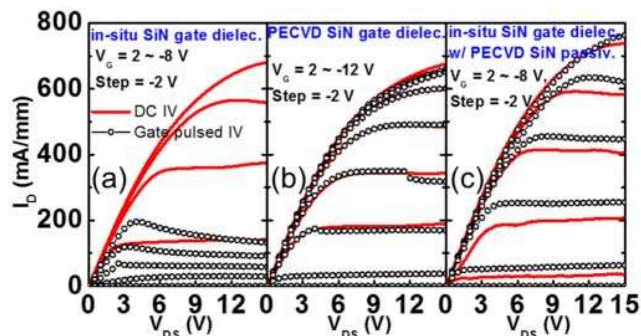

Fig. 3. DC/gate-pulsed output characteristics of the MISHEMTs with (a) *in-situ* SiN only, (b) PECVD SiN only, and (c) *in-situ* SiN gate dielectric and PECVD SiN passivation. Device dimensions: $L_G/L_{GS}/L_{GD}/W_G$ = 2/3/15/20 µm.

To further verify the effectiveness of the PECVD SiN passivation for the MISHEMTs with the *in-situ* SiN gate dielectric, a hard switching test with resistive load was performed for the devices. In this test, when the device under test (DUT) is turned off by the gate pulse, a high voltage (close to the supply voltage V_{DD}) is applied to the drain simultaneously.

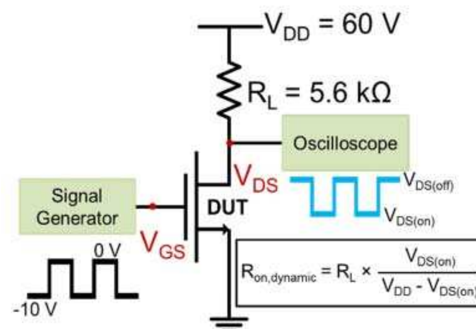

Fig. 4. Schematic of resistive load hard switching test setup. The DUT has dimensions of $L_G/L_{GS}/L_{GD}/W_G$ = 2/3/25/200 µm.

Fig.4 shows the schematic of the measurement setup, as well as the method to determine the dynamic on-resistance (R_{on}) of the DUT. The supply voltage V_{DD} is 60 V, and the load resistance R_L was determined accordingly to the bias of the DUT in the linear region at the on-state. The DUT was switched at various frequencies, ranging from 1 Hz to 1 MHz, with a duty cycle of 50%. It should be noted that, unlike the conventional double pulse measurement, the DUT in the hard switching test experiences a high-power state during the on/off switching transient. Besides the electrons trapped in the vicinity of the gate at the off-state, hot electrons can also be generated from the channel and get trapped during the semi-

on transient, which plays another role in causing current collapse [8].

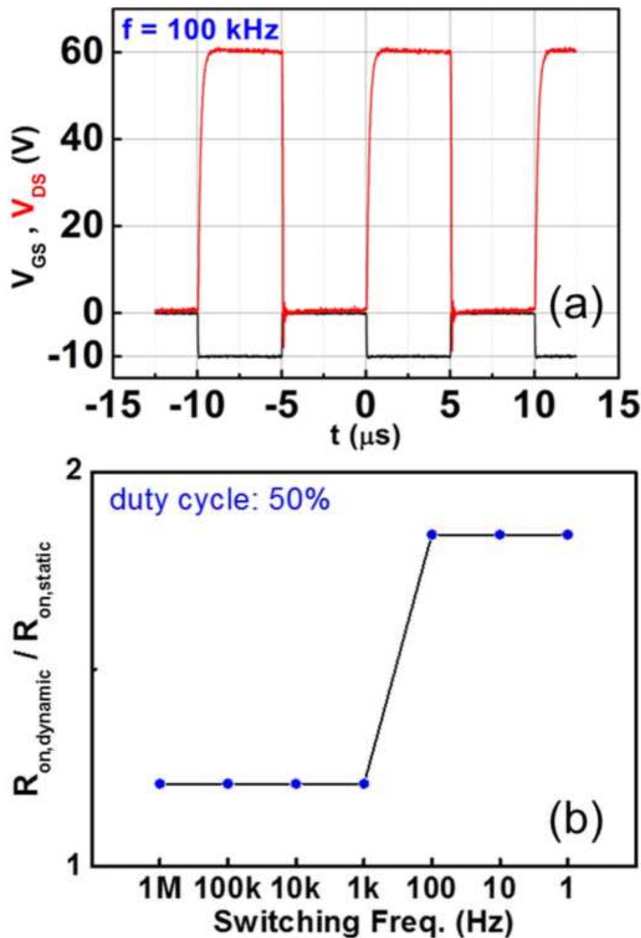

Fig. 5. (a) Switching waveform at 100 kHz for the MISHEMTs with the *in-situ* SiN gate dielectric and PECVD SiN passivation. (b) Dynamic/static on-resistance ratio under different switching frequencies.

Fig.5 (a) plots the switching waveforms of V_{GS} and V_{DS} at 100 kHz. Fig.5 (b) shows the extracted dynamic-R_{on}/static-R_{on} ratio versus various switching frequencies. Compared to the static R_{on}, only a small increase (<30%) in the dynamic R_{on} is observed with switching frequencies above 1 kHz. When switching frequencies are below 1 kHz, the slightly higher increase in the dynamic R_{on} can be ascribed to the response of some deep traps with long emission time constants (> 1 ms). The dynamic-R_{on}/static-R_{on} ratio over the switching frequencies from 1 Hz to 1 MHz is less than 2, suggesting an effective suppression of the current collapse using the bilayer passivation scheme.

CONCLUSIONS

In this paper, we have compared MOCVD *in-situ* SiN and PECVD SiN in terms of the leakage blocking capability and surface passivation effectiveness for AlGaN/GaN MISHEMTs. The MISHEMTs using an *in-situ* SiN gate dielectric exhibit two orders of magnitude lower off-state leakage than those using a PECVD SiN gate dielectric, but more severe current collapse. By combining the benefits of each type of SiN, high on/off current ratio, steep SS, and low dynamic-R_{on}/static-R_{on} ratio have been achieved simultaneously in the AlGaN/GaN MISHEMTs using an *in-situ* SiN gate dielectric with additional PECVD SiN passivation. The results suggest the great potential of using the bilayer passivation scheme in AlGaN/GaN MISHEMTs for power switching applications.

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ACRONYMS

MISHEMT: Metal-Insulator-Semiconductor High-Electron-Mobility Transistor
HEMT: High-Electron-Mobility Transistor
MOCVD: Metal-Organic Chemical Vapor Deposition
ALD: Atomic Layer Deposition
PECVD: Plasma-Enhanced Chemical Vapor Deposition
SS: Subthreshold Slope
DUT: Device under Test