Investigation of the Interface Traps and Current Collapse in LPCVD SiN_x/AlGaN/GaN MISHEMTs

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Abstract

We report on a study of AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) using low pressure chemical vapor deposition (LPCVD) SiN_x as the gate dielectric and plasma enhanced chemical vapor deposition (PECVD) SiN_x as the further passivation layer. The interface traps and current collapse in the devices were investigated by means of pulsed I-V measurements. The OFF-to-ON switching tests revealed that a bilayer LPCVD SiN_x/ PECVD SiN_x passivation scheme is distinctly effective for suppressing the current collapse.

INTRODUCTION

GaN-based metal-insulator-semiconductor high electron mobility transistors (MISHEMTs) have attracted great attraction for power switching and RF applications owing to their superior properties such as high breakdown voltage and high electron mobility. In order to enhance the MISHEMTs' gate control capability and operation stability, most recent development has focused on the gate dielectric preparation and the following dielectric/III-nitride interface quality issues. Significant progress has been made on MISHEMTs using SiN_x grown by plasma enhanced chemical vapor deposition (PECVD) or *in-situ* metal-organic chemical vapor deposition (MOCVD) [1, 2]. However, simultaneous realization of low gate leakage, large gate swing, low current collapse and high gate stability is still challenging. Very recently, low pressure chemical vapor deposition (LPCVD) SiN_x has been explored as a promising gate dielectric and passivation material for AlGaN/GaN MISHEMTs due to its high temperature and plasma-free deposition process, which can lead to high film quality and less damage on the AlGaN barrier [3, 4]. In this work, we performed a thorough study of the interface traps and current collapse in LPCVD SiN_x/AlGaN/GaN MISHEMTs using pulsed I-V measurements. It was revealed that the current collapse of the MISHEMTs could be effectively suppressed by a LPCVD SiN_x/PECVD SiN_x bilayer passivation scheme.

DEVICE FABRICATION

The AlGaN/GaN heterostructures used in this study were grown by MOCVD on a 2-in. sapphire substrate. The epi-layers consist of, from bottom to top, a 3-µm GaN buffer layer, a 1-nm AlN spacer layer and a 20-nm $Al_{0.3}Ga_{0.7}N$ barrier layer. The LPCVD SiN_x/AlGaN/GaN MISHEMT structure was schematically shown in Fig. 1.

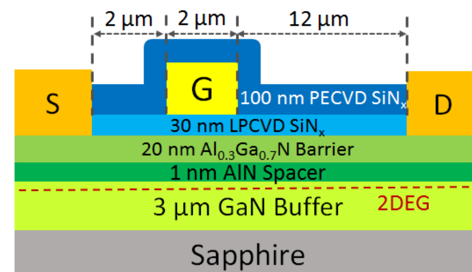

Fig. 1. Schematic diagram of the LPCVD SiN_x/AlGaN/GaN MISHEMT.

Device fabrication started from mesa isolation by a Cl_2-based inductively coupled plasma (ICP) dry etching. Then, three cycles of a digital etching process were performed immediately prior to the deposition of SiN_x by LPCVD. Each digital etching process began with UV/Ozone oxidation for 3 min and stopped with dilute hydrochloric acid (H_2O:HCl = 5:1) etching for 1 min. As the gate dielectric, 30 nm LPCVD SiN_x was deposited at 800 ℃ with a NH_3 flow of 50 sccm and a SiH_2Cl_2 flow of 16 sccm. The pressure in the LPCVD chamber is 200 mTorr and the deposition rate is about 3.3 nm/min. To prevent the GaN decomposition, NH_3 was imported into the chamber during the heating process before deposition.

After opening the contact holes, the source/drain Ohmic contacts were formed by e-beam evaporation of Ti/Al/Ni/Au based metal stack and a lift-off process, followed by an 850 ℃ anneal for 30 s in a nitrogen ambient. The gate metal was Ni/Au and the device was further passivated using 100 nm PECVD SiN_x. To make comparison, a control MISHEMT sample without PECVD SiN_x passivation was also prepared.

The MISHEMTs discussed in this paper featured a gate length (L_G) of 2 µm, a gate width (W_G) of 10 µm, a gate-to-

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drain distance (L_{GD}) of 12 μm and a gate-to-source distance (L_{GS}) of 2 μm.

Results and Discussion

Fig. 2 compares the DC output and transfer characteristics of the LPCVD SiN_x/AlGaN/GaN MISHEMTs with and without PECVD SiN_x passivation. The maximum drain current densities of both devices are around 1 A/mm at V_{DS} = 15 V and V_{GS} = 2 V (Fig. 2(a)). Compared with the MISHEMT without PECVD SiN_x passivation, the bilayer passivated device exhibited negligible hysteresis in the double-mode transfer characteristics (Fig. 2(b)). This could be attributed to the suppression of trap states that located at the MISHEMTs' access region by the PECVD SiN_x passivation.

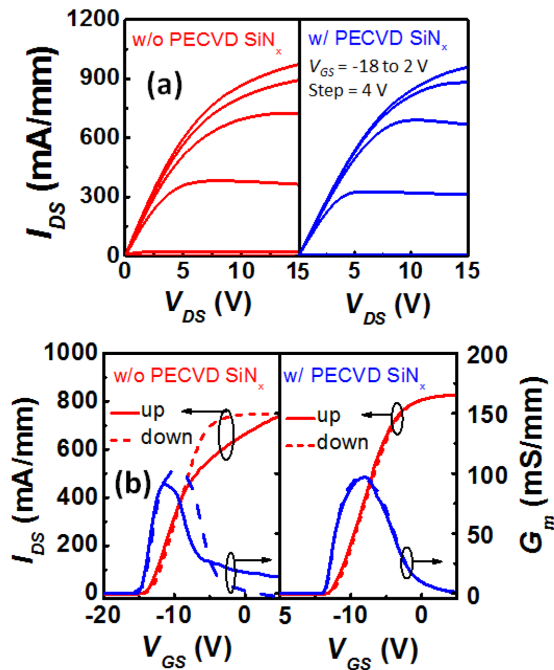

Fig. 2. (a) DC output and (b) double-mode transfer characteristics of the LPCVD SiN_x/ AlGaN/GaN MISHEMTs.

According to Fig. 3, the LPCVD SiN_x AlGaN/GaN MISHEMTs exhibited a very low gate leakage of 10^{-8} A/cm^2 at a reverse bias of -20 V and a large gate swing up to + 20 V, implying the high quality of the LPCVD SiN_x film.

The interface trap state density of the LPCVD SiN_x AlGaN/GaN MISHEMTs was analyzed using pulsed I_{DS}-V_{GS} method [5]. The pulse width (W_p) and pulse period (P_p) were 5 μs and 100 ms, respectively. V_{DS} was kept at a low value of 2 V, in order to maintain a nearly uniform occupancy of the interface traps in the gate region. In Fig. 4, the up-sweep pulsed I_{DS}-V_{GS} curve with low V_{GS_base} of -15 V was regarded as a baseline with minimal electron trapping in interface

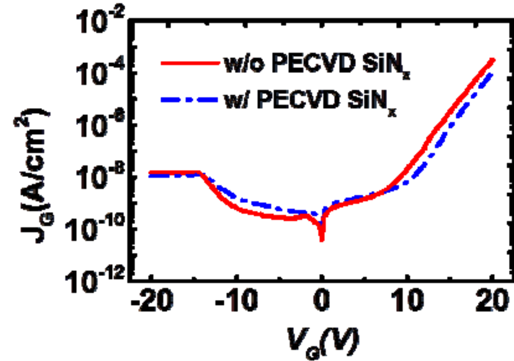

Fig. 3. Gate leakage curves of the LPCVD SiN_x/ AlGaN/GaN MISHEMTs.

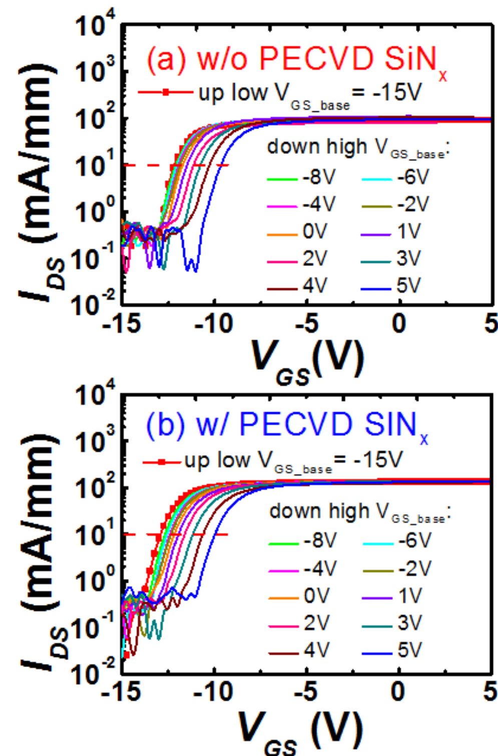

Fig. 4. Pulse-mode I_{DS}-V_{GS} characteristics at V_{DS} = 2 V. The pulse width and pulse period are 5 μs and 100 ms, respectively.

states. In the down sweep, a high V_{GS_base} was aimed at filling up the interface states below the Fermi level corresponding to the high V_{GS_base}, resulting in the hysteresis of the pulsed I_{DS}-V_{GS} curve. Interface states with time constants shorter than W_p = 5μs would emit electrons before each measurement point and thus could not be detected using this pulsed I_{DS}-V_{GS} method. The detectable energy range could be deduced from the Shockley-Read-Hall statistics

$$\tau_e = \frac{1}{\upsilon_{th}\sigma_n N_C}\exp\left(\frac{E_C - E_T}{kT}\right) \quad (1)$$

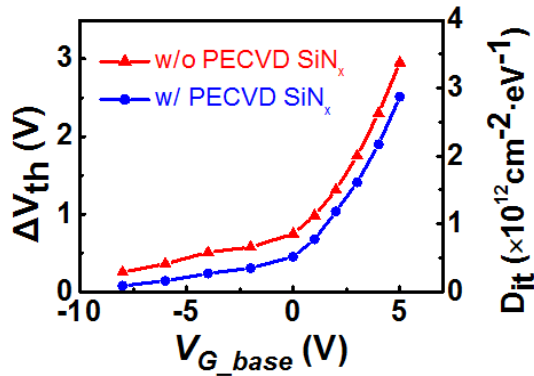

Fig. 5. ΔV_{th} and D_{it} extracted from the pulse mode I_{DS}-V_{GS} measurements.

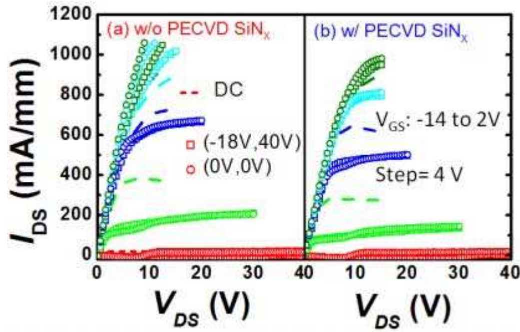

Fig. 6. Pulsed I_{DS}-V_{DS} characteristics (with the DC reference) measured from two quiescent bias points of (V_{GSQ}, V_{DSQ}) = (-18 V, 40 V) and (0 V, 0V).

where v_{th}, σ_n and N_C are the electron thermal velocity, electron capture cross section and electron concentration at the effective density of states in the conduction band in GaN, respectively [5, 6]. In this work, the detectable energy range was calculated to be E_C-$E_T \geq 0.38$ eV.

The interface trap density D_{it} could be determined by

$$D_{it} = \frac{C_{OX} \cdot \Delta V_{TH}}{q^2} \quad (2)$$

where C_{OX} = 192 nF/cm^2, and ΔV_{TH} is the hysteresis extracted from the pulsed I_{DS}-V_{GS} curves in Fig. 4.

Fig. 5 plots the hysteresis and the interface trap state density as a function of V_{GS_base}. The small difference of D_{it} between the MISHEMTs with and without PECVD SiN_x passivation suggested that the PECVD SiN_x layer has less influence on the trap states in the MISHEMTs' gate region.

To further evaluate the current collapse quantitatively, pulsed I_{DS}-V_{DS} measurements were performed for both samples [7]. Fig. 6 illustrates the pulsed I_{DS}-V_{DS} curves measured from two quiescent bias conditions of (V_{GSQ}, V_{DSQ}) = (-18V, 40V) and (0V, 0V). The negligible difference observed in the linear region of the pulsed I_{DS}-V_{DS} curves for the bilayer SiN_x passivated MISHEMT suggested a low current collapse, while the unpassivated device showed obvious current collapse.

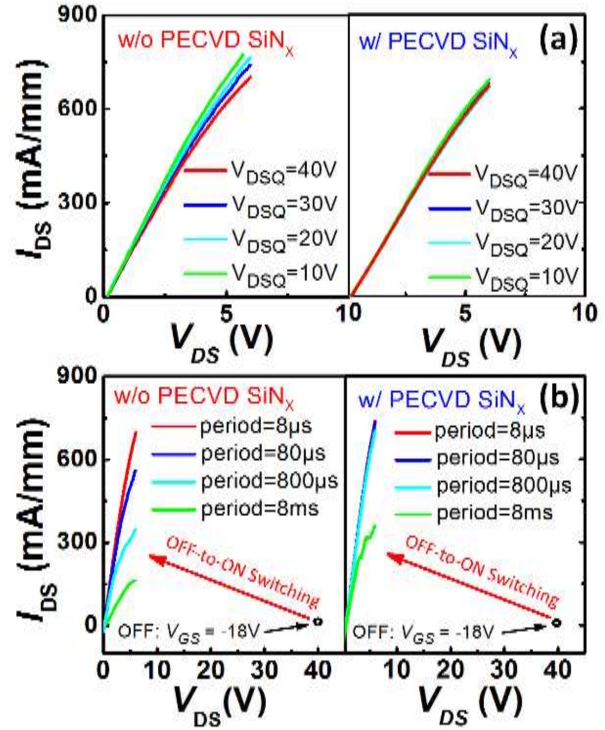

Fig. 7. OFF-to-ON switching tests with various OFF-state V_{DSQ} (a) stress from 10 to 40 V and (b) stress period from 8 μs to 8 ms.

The transient OFF-to-ON switching characterizations were performed for the fabricated MISHEMTs. As shown in Fig. 7(a), the devices were switched from the OFF state with a quiescent gate bias of -18 V and a quiescent drain bias of 10−40 V (10 V step) to the ON state with a gate bias of 2 V. The applied pulse width and period are 0.8 μs and 8 μs, respectively. Dynamic R_{ON} was extracted from the linear regime (V_{DS}: 0 to 6 V) of the pulsed output curve. For the passivated MISHEMT, the pulsed output curves with various OFF-state drain biases were highly overlapped, while evident dispersion was observed among the curves for the unpassivated device.

Fig. 7(b) shows the pulsed output curves under a 40-V OFF-state drain bias with various OFF-state V_{DSQ} stress periods from 8 μs to 8 ms. For the passivated MISHEMT, the dynamic R_{ON} with a stress period of 800 μs remained as low as only 1.04 times of the one with a stress period of 8 μs. By contrast, the ratio with the same measurement conditions for the unpassivated device was 2.10. In addition, the passivated MISHEMT exhibited much lower dynamic R_{ON} degradation even with a stress period of 8 ms. The low current collapse in the bilayer SiN_x passivated MISHEMT could be attributed to the shallow donor-like traps existing at the SiN_x/III-Nitride interface, which could modify the surface potential and inhibit electron injection from gate into surface states [8, 9].

CONCLUSIONS

We have investigated the interface traps and current collapse in LPCVD SiN_x/AlGaN/GaN MISHEMTs. Small gate leakage current, large gate swing and low interface trap state density demonstrated the feasibility of using LPCVD SiN_x as gate dielectric for AlGaN/GaN MISHEMTs. Moreover, an LPCVD SiN_x/PECVD SiN_x bilayer passivation scheme has been developed for the MISHEMTs to suppress the current collapse, leading to enhanced dynamic performance.

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ACRONYMS

MISHEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor

LPCVD: Low Pressure Chemical Vapor Deposition

PECVD: Plasma Enhanced Chemical Vapor Deposition

MOCVD: Metal-Organic Chemical Vapor Deposition

ICP: Inductively Coupled Plasma