A SiN Passivation for Improved Moisture Reliability of Au Interconnect With Low-K BCB ILD

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Abstract

Low-k interlevel dielectrics, such as BCB, have found applications in high performance GaAs devices such as HBTs and passives, especially as a planarizing layer. These ILDs themselves are not completely moisture resistant, and often require more moisture resistant dielectrics such as SiN or oxy-nitride around the metallization and or over the BCBs to properly seal devices.

Good quality SiN films for GaAs devices are deposited in plasma enhanced chemical vapor deposition systems, in temperature ranges between 200C and 350C. Unfortunately, due to high thermal expansion coefficient mismatches between the ILD, the nitride, and the gold metallization, cracks are often observed in the SiN dielectrics, particularly at corner regions of BCB, Au and SiN. Stress management is required to avoid these cracks and improve moisture reliability. In temperature and humidity environmental tests, moisture penetration through seams, and cracks in dielectrics may result in corrosion of the structure, leading to leakage fails [1, 2].

A passivation scheme using a periodic multi-layer of SiN with compressive and tensile films, with net compressive stress, was developed for nitride deposited over BCB, and Au interconnect, which mitigated crack formation. This passivation scheme, in particular with an additional SiN low stress hardmask interfacing the BCB, significantly improved moisture reliability for HBTs and passive components as evaluated in environmental tests of THBL, BHAST, and PCT.

INTRODUCTION

Exceptional moisture reliability of devices for high volume handset applications is desired in the market. The observation of low levels of moisture reliability fails in our first generation HBTs was a concern, and we embarked on a project to improve reliability. Failure analysis of the devices failing temperature, humidity, bias and life reliability tests (THBL) indicated the integrity of passivation scheme using low-k BCB ILDs and low stress SiN layers over the BCB and around M2 structures, was inadequate in fully sealing the devices. Under highly accelerated biased humidity testing [3], sporadic corrosion and humidity-induced metal migration was observed. Failure analysis indicated many cracks at the corners of M2, BCB-ILD, and the SiN, a potential path for moisture ingress. This is illustrated in the schematic of the interconnect, and an SEM cross-section in Figures 1, and 2.

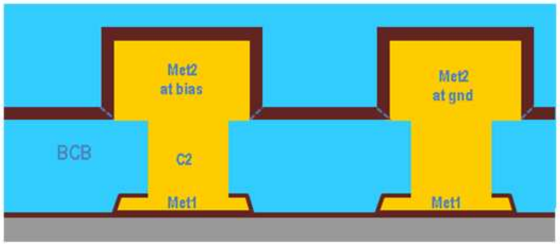


Figure 1. Schematic of 2-metal layer HBT Interconnect using low-K BCB ILD and overcoat and SiN dielectrics, showing possible crack locations in final SiN passivation.

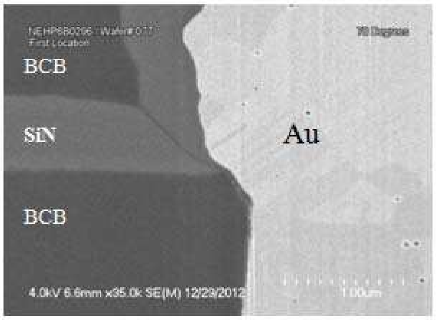


Figure 2. SEM cross-section of passivation of Au interconnects with BCB ILD and overcoat with crack development in the SiN final passivation.

The passivation on top of BCB and around M2 was low compressive stress silicon nitride. We suspected thermal expansion coefficient mismatch of the BCB, Au and SiN was responsible for the cracks in the nitride (Table 1). The HBT device uses an InGaP / GaAs epitaxial structure. The high topography is planarized with the first BCB ILD spin-coated and cured. Two layers of interconnect metallization of evaporated M1 and plated M2 of 1um and 4um gold respectively, are used. An overcoat BCB is also provided after the final nitride passivation layer.

Table 1 shows the thermo-mechanical properties of Au, BCB and SiN.

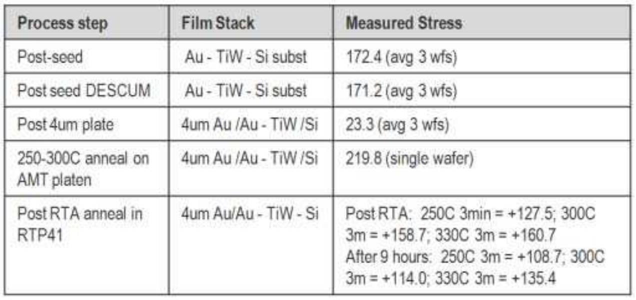
Table 1. Thermo-mechanical properties

Material	Density (kg/m^3)	CTE (1/degK)	E (Pa)	v	Heat Capacity Cp(J/kg.degK)	Thermal Conductivity (W/m.deg)
Au	19300	14.2E-6	70E9	0.44	129	317
BCB	950	42E-6	2.9E9	0.3	258.5+3.368*T	0.29
SiN	3186	3.2E-6	310E9	0.27	700	30

INITIAL INVESTIGATION OF STRESS EFFECT

Stresses in the plated gold, BCB and nitride were measured separately by deposition on silicon. Stress in the plated gold interconnect layer was found to be set fundamentally by the downstream annealing temperature, rather than the as-deposited plating stress. Stresses were measured stepwise in the seed metallization, post seed descum, after 4um Au plating, after anneal between 250C and 300C, and then subsequently in an RTA system (Table 2). The stresses are tensile.

Table 2 . Stress Measurements on Plated Gold in Mega Pascal



Process step	Film Stack	Measured Stress
Post-seed	Au - TiW - Si subst	172.4 (avg 3 wfs)
Post seed DESCUM	Au - TiW - Si subst	171.2 (avg 3 wfs)
Post 4um plate	4um Au /Au - TiW /Si	23.3 (avg 3 wfs)
250-300C anneal on AMT platen	4um Au /Au - TiW /Si	219.8 (single wafer)
Post RTA anneal in RTP41	4um Au/Au - TiW - Si	Post RTA: 250C 3min = +127.5; 300C 3m = +158.7; 330C 3m = +160.7 After 9 hours: 250C 3m = +108.7; 300C 3m = +114.0; 330C 3m = +135.4

A simple estimation from the thermal expansion mismatch of gold and silicon, will predict gold stresses on the order seen in the measurements of 165-215 MPa.

$$\sigma_{Au} = \frac{E_{Au}}{1-\upsilon_{Au}}(CTE_{Au} - CTE_{Si})\Delta T \text{ .... } [1]$$

$$\vartheta = 0.33 \text{ .... } [2]$$

$$\sigma_{Au} = 187\ MPa \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots [3]$$

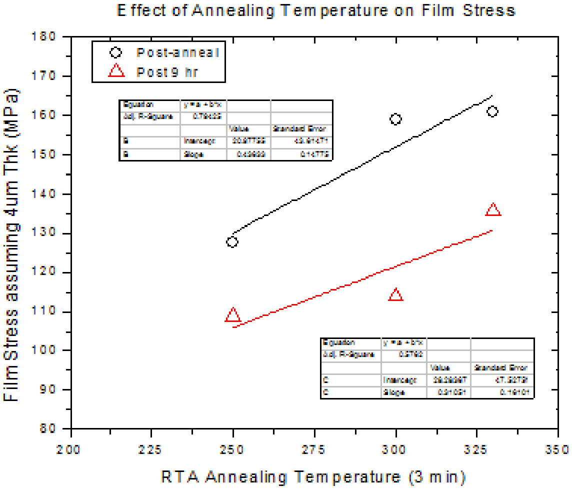


Figure 3. Effect of Rapid Thermal Annealing Temperature on Plated Gold Stress.

Cracks occur at the corners of BCB, Au and SiN because during deposition, a high enough stress is generated in the gold and together with the high strains due to the BCB, the gold contracts widthwise, and expands in the height direction, by virtue of Poisson ratio. This contraction and expansion leads to cracks in the SiN dielectric at the corners, if the SiN dielectric has low compressive stress. Increasing the compressive stress in the SiN reduces the expansion effect of Au in the vertical direction preventing cracks. A COMSOL transient simulation result is shown in Figures 4, 5, where the structure in Figure 4A is heated to 300C, held for a few minutes and rapidly cooled to 25C in 1 minute.

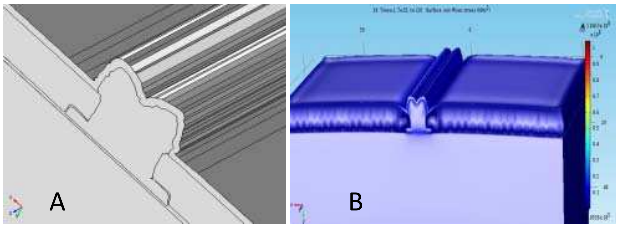


Figure 4. (A) Cross-section of an Au M1 and M2 interconnect with SiN final passivation on the BCB ILD for COMSOL simulation. (B) Transient simulation results, heating to 300C for 3 mins, and cooling to 25C in a minute. Initial SiN Stress= -50 MPa, Gold stress= 0 MPa, BCB=0 MPa.

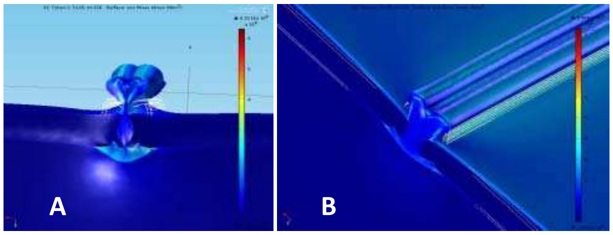
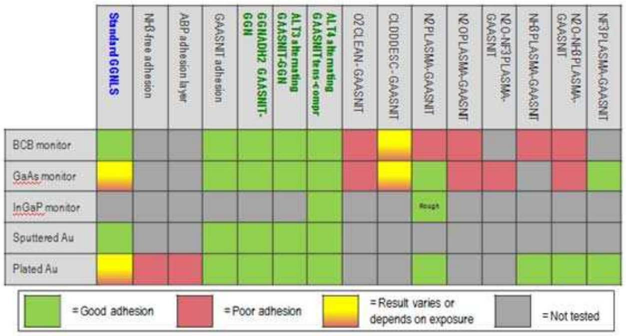


Figure 5. (A) COMSOL simulation results with initial stresses SiN=-50 MPa, Au=218 MPa, BCB=0 Mpa (B) COMSOL simulation results with Initial SiN Stress= -400 MPa, Gold stress= 218 MPa, BCB=0 MPa.

PERIODIC MULTI-LAYER SiN DEVELOPMENT

To improve passivation integrity of the HBT technology that uses BCB ILDs, good quality dielectric film with good adhesion to gold, and BCB were needed. Also the stress in the SiN had to be highly compressive to mitigate cracks. Since thick SiN highly compressive films were known to be prone to cracking from other non-BCB technologies, we decided to evaluate multilayer films with alternating compressive and tensile films. Adhesion tests were performed by tape-pull test, and nitride films fabricated between 250C and 300C, without He in the gas (called GAASNIT) were found to be best regarding adhesion. A number of pre-cleans of the BCB and gold prior to SiN deposition were also investigated. Table 3 summaries the finding. Different versions of nitride are listed in the table. ALT3 and ALT4 refer to alternating compressive and tensile GAASNIT of different effective stress. GGN is a low compressive stress nitride using mixtures of NH3/He and SiH4 in deposition. ABP nitride is a highly tensile nitride, also with NH3/He mixtures. GGNADH2E is a graded nitride between GAASNIT and GGN.

Table3. Nitride Adhesion Studies



	Standard GGNLS	NH3-free adhesion	ABP adhesion layer	GAASNIT adhesion	**GGNADH2 GAASNIT-GGN**	**ALT3 alternating GAASNIT-GGN**	**ALT4 alternating GAASNIT tens-compr**	O2 CLEAN-GAASNIT	CLDDESC-GAASNIT	N2PLASMA-GAASNIT	N2OPLASMA-GAASNIT	N2O-NF3PLASMA-GAASNIT	NH3PLASMA-GAASNIT	N2O-NH3PLASMA-GAASNIT	NF3PLASMA-GAASNIT
BCB monitor	🟩	▨	▨	🟩	🟩	🟩	🟩	🟥	🟨	🟥	🟥	▨	🟥	🟥	▨
GaAs monitor	🟨	▨	▨	🟩	🟩	🟩	🟩	🟥	🟨	🟩	🟥	🟥	▨	🟥	🟩
InGaP monitor	▨	▨	▨	▨	▨	▨	🟩	▨	▨	🟩 Rough	▨	▨	▨	▨	▨
Sputtered Au	🟩	▨	▨	🟩	🟩	🟩	🟩	▨	▨	▨	▨	▨	▨	▨	▨
Plated Au	🟨	🟥	🟥	🟩	🟩	🟩	🟩	▨	▨	🟩	▨	▨	🟩	🟩	🟩

🟩 = Good adhesion
🟥 = Poor adhesion
🟨 = Result varies or depends on exposure
▨ = Not tested

Two other proxy techniques used to assess integrity were a KII etch for 60 minutes, and evaluation of etch pits through the dielectric, as well as 96 hour PCT or pressure cooker test (121 C, 100% RH) to look for delaminations.

Various films of different effective stresses were investigated shown in Figure 6. The more compressive films with effective stress >400 MPa were better and had no cracks, or KII attacks.

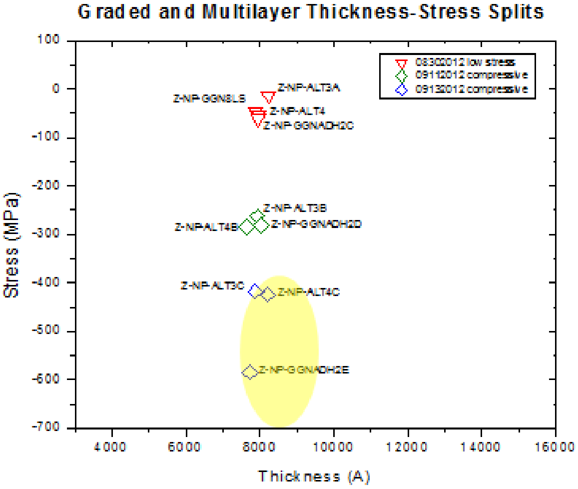


Figure 6. Graded and Multilayer film stress of various total thicknesses.

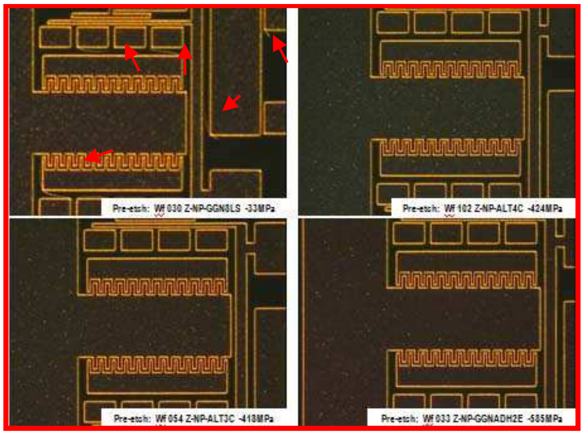
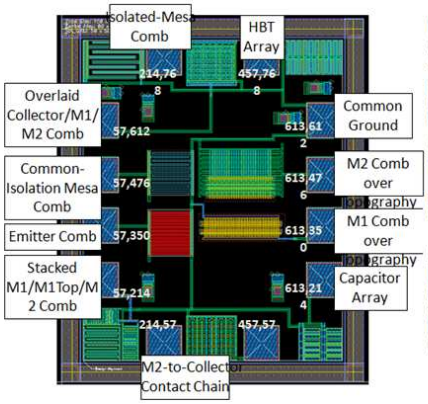


Figure 7. Cracks indicated by red arrows are common on the low stress GGN sample. Cracks are nearly completely absent on the 4-600MPa compressive films.

Figure 8. A KII etch for 1 hour shows the low stress GGN films seriously attacked, whereas highly compressive films are not attacked.

MOISTURE RELIABILITY

Moisture reliability was investigated with a moisture-resistance monitor MRM test structure as well as MMIC circuits. PCT was performed on wafers to evaluate dielectric delamination. Figure 9 is the MRM test structure and completed HBT wafers were diced and MRM packages and MMIC packages were subjected to THBL at 85 °C /85% RH for about 1000 hours.



Intended for a single positive DC bias to be applied to all pads except the common ground during moisture stress. Testing leakage of each structure's bias pad to ground should identify affected devices.

Frame size is 750x905um Pad openings 80x80um

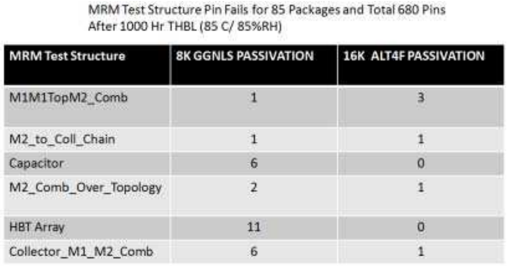
Coordinates indicate the lower left corner of each pad Pcell in microns with respect to origin at lower left of design (with 80x80um frame included).

Figure 9. MRM test structure with various test structures for leakage after environmental stress.

RELIABILITY RESULTS AND FURTHER PASSIVATION IMPROVEMENTS

The MRM test structures and MMIC circuits showed improvement in the moisture reliability using thick alternating tensile/compressive stress dielectric referred as ALT4F. This had an effective compressive stress of -450 MPa. The multilayer dielectrics are deposited from tensile and compressive films of GAASNIT typically 200-800A individual film thickness each, and periods 5 to 10. Deposition chemistry and conditions were adjusted to calibrate stress. Tables 4 and 5 are test results. A voltage of 4.2 V was applied and parts with leakages exceeding 20 nA were deemed failed.

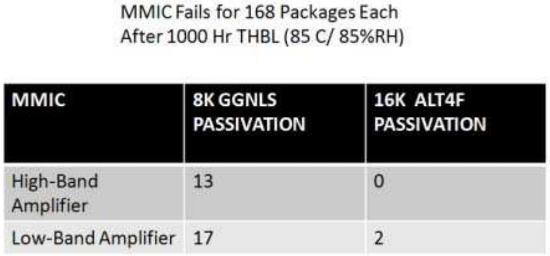
Table 4.



MRM Test Structure Pin Fails for 85 Packages and Total 680 Pins
After 1000 Hr THBL (85 C/ 85%RH)

MRM Test Structure	8K GGNLS PASSIVATION	16K ALT4F PASSIVATION
M1M1TopM2_Comb	1	3
M2_to_Coll_Chain	1	1
Capacitor	6	0
M2_Comb_Over_Topology	2	1
HBT Array	11	0
Collector_M1_M2_Comb	6	1

Table 5.



MMIC Fails for 168 Packages Each
After 1000 Hr THBL (85 C/ 85%RH)

MMIC	8K GGNLS PASSIVATION	16K ALT4F PASSIVATION
High-Band Amplifier	13	0
Low-Band Amplifier	17	2

Further improvement of the passivation was realized by inserting a low stress nitride layer immediately on the as-deposited and cured BCB, and re-integrating the interconnect module to retain this layer in the final product, Figure 10.

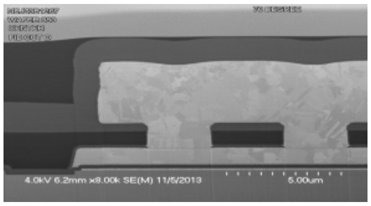


Figure 10. Integration of a secondary low stress SiN on BCB with ALT4F multi-layer final passivation [4].

The benefit of this additional passivation layer is two-fold: first, it provides additional hermetic layer in the product; second, it greatly promotes adhesion of downstream nitride stacks to the first BCB ILD. Table 6 shows reliability results of MMIC amplifier based on this version.

Table 6. THBL and BHAST results of MMIC circuits. The GGNLS process was improved by incorporating adhesion improvements. The BHAST results with alternating ALT4F film with secondary passivation achieved the best reliability results.

RELIABILITY TEST ON MMIC AMPLIFIER	TEST POINT	GGNLS PASSIVATION	BEST CASE 16K ALT4F WITH 5K SECONDARY LOW STRESS NIT on BCB
THBL 85C /85% RH Vcc=4.2V	504 hrs	0/60	0/60
	1000 hrs	0/60	0/60
BHAST 130 C /85% RH Vcc=4.2 V	48 hrs	0/48	0/48
	96 hrs	1/48	0/48
	144 hrs	2/48	0/48

CONCLUSIONS

A multi-layer SIN passivation scheme of compressive, and tensile films, and a secondary low stress SiN directly on BCB ILD were developed to improve moisture reliability of HBT MMICs.

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ACRONYMS

ILD	Interlevel Dielectric
THBL	Temperature Humidity Bias Life
BHAST	Bias Humidity Accelerated Stress Test
BCB	Benzo-cyclo-butane
AVI	Automatic Visual Inspection
PCT	Pressure Cooker Test commonly known as Autoclave