Investigation of InAlN/GaN Schottky Barrier Diode (SBD) on 6-inch SOI Substrate

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Abstract

The low frequency noise and reverse recovery time characteristics of 6 inch InAlN/AlN/GaN Schottky barrier diode (SBD) were demonstrated and investigated on silicon-on-insulator (SOI) substrate for the first time. The Raman spectroscopy measurement indicates that the smaller epitaxy stress was obtained by adopting SOI wafer and X-ray diffraction measurements revealed that InAIN SBD on SOI achieves a flat surface and an abrupt hetero interface. Based on the DC and low frequency noise (LFN) measurement at various temperatures ranging between 300 and 450 K, the InAlN/GaN SBD on SOI design shows better forward current and reverse current, and the InAlN/GaN SBD on SOI design achieved a lower reverse recovery charge.

INTRODUCTION

InAlN/GaN heterostructures have demonstrated a great potential in high-speed and high-power electronics due to their high device breakdown voltage and high current density [1], which are two key factors in high power switching applications such as converters and inverters, including solid-state drives for motors and electrical vehicles. In addition, the InAlN barrier layers offers a potential solution to the strain problem, because the $In_xAl_{1-x}N$ alloy can be lattice-matched to GaN, potentially resulting in better device reliability than AlGaN/GaN heterostructures especially under high voltage and high temperature environments [2]. One of the GaN devices, the GaN Schottky barrier diode (SBD), has attracted tremendous attention for its high breakdown voltage, low on-resistance, and rapid reverse-bias recovery [3-5]. Recently, 6 inch or 8 inch silicon (111) substrates were selected as an epitaxial growth substrate for GaN power electronic devices because of their low cost and the superior scalability of the wafer [6-7]. However, InAlN/GaN SBD on Si substrate suffers from the disadvantages that electrical breakdown occurs vertically through the silicon substrate and the lossy substrate sacrifices the device operation bandwidth. In this letter, we successfully fabricated InAlN/GaN Schottky barrier diodes on (100) Si-SiO_2-(111) Si silicon-on-insulator (SOI) substrate, and we obtained better device characteristics by DC measurement, low frequency noise measurements, and reverse recovery measurements.

DEVICE STRUCTURE AND FABRICATION

Fig. 1(a) shows the cross-sectional schematic and scanning electron microscope (SEM) profile of the InAlN/AlN/GaN Schottky barrier diode, grown by MOCVD system on a 6-inch SOI substrate. The thickness of the p-type (111) Si layer was 5 μm and the buried SiO_2 is 0.5 μm. This SOI substrate design is beneficial for heterogeneous integration with Si (100) CMOS-compatible technology by removing the top material, including GaN, (111) Si, and SiO_2 [8]. A 2 μm-thick GaN layer was grown on top of a 1.2 μm-thick AlGaN/AlN buffer/transition layer. A 1 nm-thick AlN spacer layer was sandwiched between the GaN channel layer and the 10 nm-thick $In_{0.17}Al_{0.83}N$ Schottky layer to increase the carrier concentration and mobility in the two dimensional electron gas (2-DEG). Finally, a 10 nm GaN cap layer was grown to prevent the oxidation of InAlN caused by moisture. All of the layers are unintentionally doped. For comparison, the identical epitaxy structure was also grown on a high resistivity (HR, >6000 $\Omega \times cm$) Si substrate. The two dimensional electron gas (2-DEG) sheet carrier density and the mobility of the InAlN / GaN on SOI substrate were 1.91×10^{13} cm^{-2} and 1225 cm^2/V-sec at 300 K, compared to 1.81×10^{13} cm^{-2} and 1270 cm^2/V-sec for InAlN/GaN on HR-Si substrate, respectively. For SBD device fabrication, the active regionwas protected by a photoresist and the mesa isolation region was accomplished with inductively coupled plasma etching using BCl_3, Cl_2, and Ar. Ohmic contacts were prepared by electron beam evaporation of a multilayered Ti/Al/Ni/Au (30 nm/125 nm/ 50 nm/200 nm) sequence, followed by rapid thermal annealing at 850◦C for 30 s in a nitrogen-rich ambient. The ohmic contact resistance is 8.6×10^{-6} $\Omega \cdot cm^2$, as measured by the transmission-line method. The 20 μm long anode terminals with 100 μm width was formed by Ni/Au (10/500 nm) evaporation and subsequent lift-off process. Finally, a 200 nm-thick SiO_2 layer was deposited as a final passivation layer with the interconnection formed by a Ti/Au (30 nm/1000 nm) metal layer.

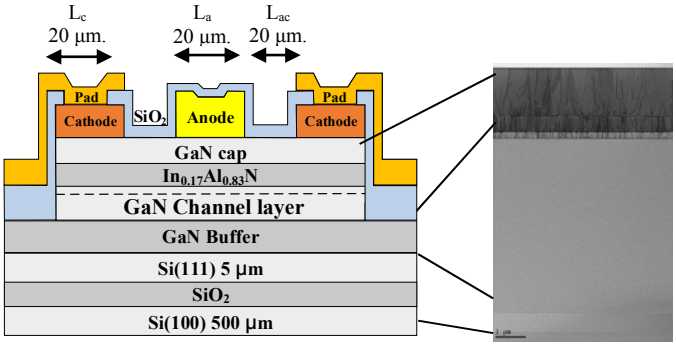

Fig.1 (a). Device structure and cross-section of InAlN/GaN schottky barrier diode with a L_a = 20 µm, L_c = 20 µm and L_{ac} = 20 µm.

RESULTS AND DISCUSSION

Fig. 2(a) shows 2θ-ω X-ray diffraction (XRD) profiles for InAIN/AlN/GaN heterostructures on SOI and HR-Si substrate, respectively. The curves of these two samples have clear InAIN, GaN, AlN peaks and fringes, which means that the samples have flat surfaces and abrupt heterointerfaces. In order to guarantee the stress release phenomenon of 6 inch SOI substrate caused by large lattice mismatch between GaN/Si interface, the Micro-Raman spectroscopy was performed on both wafers. As shown in Fig. 2(b), the E2 peak of device on SOI substrate was found to be 568 cm^{-1} and measured results is similar to the standard freestanding GaN film value (567.4 cm^{-1}). As compared to the device on HR-Si substrate (566.5 cm^{-1}), an obvious tensile stress in the GaN was observed for the devices on HR-Si substrate and the device on SOI substrate exhibits a better stress release performance. This is beneficial for improving long-term operational reliability.

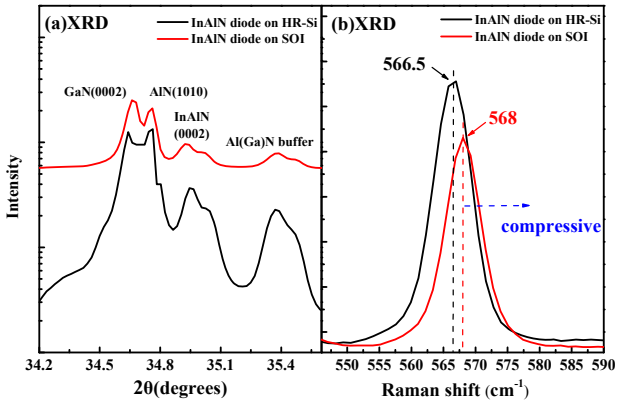

Fig. 2(a) 2θ-ω X-ray diffraction (XRD) profiles for InAIN /GaN on SOI and HR-Si substrate, (b) Micro-Raman spectroscopy was performed on both wafers.

Fig. 3 shows the typical forward I–V characteristics of the InAlN/GaN SBD on SOI as well as those of the conventional InAlN/GaN SBD on HR-Si at 300K and 450K environments. The InAlN SBD on SOI has the lower turn-on voltage of 0.55 V, defined at a current density of 10 A/cm^2 normalized to the active area including the anode and the cathode contacts. In contrast, the turn-on voltage for the InAlN SBD on HR-Si is 0.7V, obtain a low on-voltage due to InAlN / GaN on SOI had a better stress release to reduce the scattering effect and defects,. During the SBD turn-on operation, the series resistance is 5.26 mΩ·cm^2 for InAlN/GaN SBD on HR-Si and this value was 3.6 mΩ·cm^2 for the InAlN/GaN SBD on SOI. Fig. 3 also indicated that temperature increase from 300 K to 450 K results into a current degradation of 54.4% for InAlN/GaN SBD on HR-Si and versus 35.5 % for InAlN/GaN SBD on SOI. Since an SOI substrate reduces electron scattering in the channel, so InAlN/GaN on SOI also has better performance in high temperature.

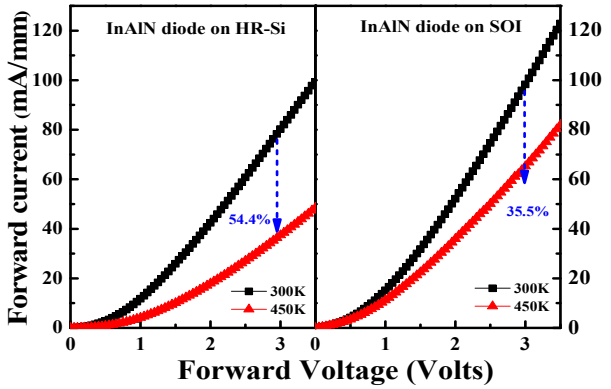

Fig. 3 Typical forward I–V characteristics of the InAIN /GaN on SOI and HR-Si substrate

Fig. 4 shows the breakdown characteristics of these two SBDs and both of them showed sharp breakdown characteristics. The measured breakdown voltage of the proposed InAlN/GaN SBD on SOI was 395 V, while that of the conventional InAlN SBD on HR-Si was 371 V, and also it shows the SOI substrate effectively inhibit reverse leakage current.

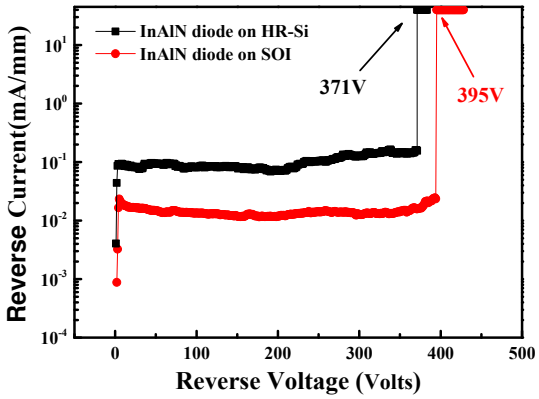

Fig. 4 breakdown characteristics of the InAIN /GaN on SOI and HR-Si substrate

In order to further study the buffer interface trapping and InAlN barrier layer of both devices, the 300 K and 450 K low frequency noise spectra were measured. Obviously, both devices performed a similar interface trapping noise at 450 K operation. However, the LFN of InAlN SBD on HR-Si was increased by one order of magnitude because the Silicon substrate has the problem of poor stress and the carrier scattering induced noise was also enhanced. Comparatively speaking, InAlN/GaN SBD on SOI showed a smaller increase in noise with increasing temperature, resulting in the lower LFN at 450 K operation show in Fig 5. Fig. 6 shows the reverse recovery characteristic of the InAlN/GaN SBD when the diode was switched from forward (I_F = 1 A) to reverse bias (-30 V) with dI/dt of 60 A/μs. The reverse recovery effect was still observed due to the parasitic capacitance of the Schottky diode. The calculated reverse recovery charge Q_{rr} depends on several factors: the diode junction capacitance, the concentration of deep levels in the bandgap, and the parasitic capacitances shunt to the Schottky diode. Table.1 shows that the Q_{rr} of the InAlN/GaN SBD on SOI was smaller than that of the InAlN SBD on HR-Si. From the previous characteristics show the SOI substrate improved the concentration of deep levels in the bandgap.

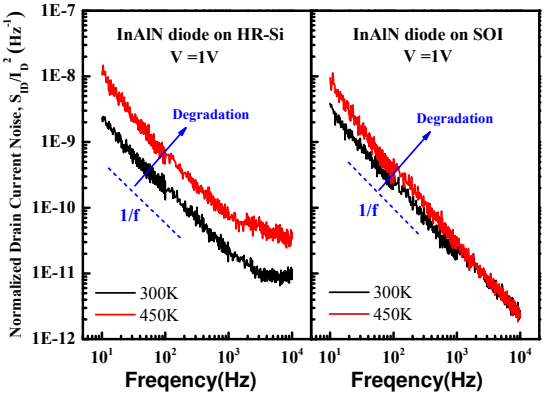

Fig.5 The flicker noise spectra characteristics of the InAIN /GaN on SOI and HR-Si substrate from 300K to 450K at V = 1 V

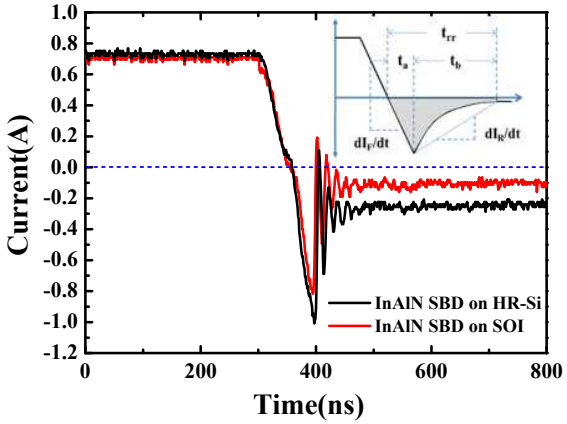

Fig.6 The reverse recovery characteristics of the InAIN /GaN on SOI and HR-Si substrate (Inset define the T_a 、T_b 、T_{rr} area)

Table1. The reverse recovery measurement data

Device	IRM (A)	Ta (ns)	Tb (ns)	Trr (ns)	Qrr (nC)
InAlN diode on HR-Si	-0.99	16.0	2.4	18.4	10.26
InAlN diode on SOI	-0.81	15.6	2.4	18.0	6.91

CONCLUSION

In this letter, we have demonstrated InAlN/GaN Schottky barrier diodes on SOI substrate. Based on the DC and LFN measurement at various temperatures ranging between 300 and 450 K, the InAlN/GaN SBD on SOI design shows better forward current and reverse current due to the SOI substrate exhibits a better stress release performance, According to the reverse recovery time measurement, the InAlN/GaN SBD on SOI substrate achieved a lower reverse recovery effect and improved epitaxial quality which are key advantages for this proposed device performed the very good switching properties and the potential to operate at very high switching frequencies and high temperatures (up to 450 K) with low switching loss.

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ACRONYMS

HEMT: High electron mobility transistor
GaN: Gallium Nitride
SOI: Silicon On Insulator