Low Distortion Tunable RF Components, a Compound Semiconductor Opportunity

Cong Huang[1], Koen Buisman[1], Peter J. Zampardi[2], Lis K. Nanver[1],
Lawrence E. Larson[3] and Leo C. N. de Vreede[1]

[1]Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft University of Technology,
Mekelweg 4, 2628 CD, Delft, the Netherlands, c.huang@tudelft.nl, 0031(0)152787964
[2]Skyworks Solutions, Inc., 2427 W. Hillcrest Drive 889-A1, Newbury Park, CA 91320
[3]Center for Wireless Communications, Department of Electrical and Computer Engineering,
University of California at San Diego, 9500 Gilman Drive, La Jolla, CA 92093-0407

Keywords: Compound semiconductor, low distortion, Q factor, tunable circuits and devices, varactors.

Abstract

An overview is given for the current state-of-the-art of semiconductor based tunable RF elements. For this purpose, semiconductor based capacitive switch banks and varactors are reviewed and compared with the recently developed ultra-low distortion semiconductor based varactors. It reveals that the latter solution, when compared against all existing technology platforms for continuously tunable elements, can provide superior performance in tuning range, linearity, and quality factor.

INTRODUCTION

With the development of wireless communication, tunable elements like continuously variable reactors (varactors) and capacitive switch banks can play an important role to facilitate RF reconfigurability and phase-diversity systems. Application examples include: adaptive matching for multi-band/multi-mode power amplifiers and antenna mismatch correction, tunable filters, as well as adjustable "true" time delay phase shifters for smart antenna systems.

An ideal tunable RF element for these applications will exhibit very low loss, low DC power consumption, high linearity, excellent ruggedness to high voltage and high current conditions, large tuning range, high reliability, low cost, low area usage, and will be continuously tunable with high tuning speed.

Compared to MEMS solutions, semiconductor based counterparts provide advantages in terms of low control voltage, high capacitance density, low packaging costs, high reliability and technology compatibility. Within this work, conventional semiconductor based capacitive switch banks and varactors are reviewed for their benefits and shortcomings and compared with the recently developed ultra low-distortion semiconductor based varactors.

CAPACITIVE SWITCH BANKS AND CONTINUOUSLY TUNABLE VARACTORS

Theoretically, an ideal switch exhibits an "open" in the OFF state and "short" in the ON state. When such a switch is series connected with a fixed capacitor (C_{fix}), a capacitive switch is created, which can alternate between an "open" and a fixed capacitance value (C_{fix}). By combining N capacitive switches as shown in Fig. 1(a), a capacitive switch bank is created, which can provide 2^N different capacitance values. These types of capacitive switch banks typically provide only discrete tuning resulting for applications that require fine tuning, in a high number of capacitive switches with related control voltages. In contrast, tunable varactors [Fig. 1(b)] provide continuous capacitance tuning over a given range with only one control voltage. Generally speaking, the first solution is better suited to implement high capacitance tuning ranges, under the assumption that an excellent switch is available, whereas continuously tunable varactors can offer a more favorable combination of quality factor and tuning resolution. Both candidates are subject to intensive research to reduce their device parasitics in order to achieve an improved quality factor and capacitance tuning range.

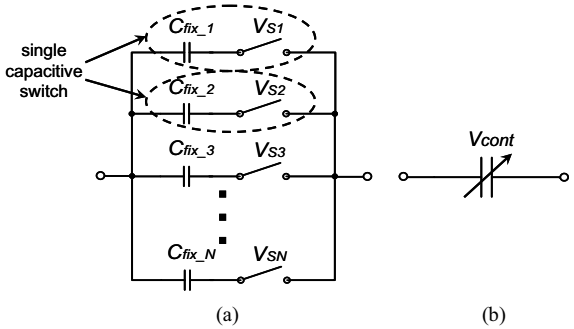

Fig. 1. (a) Schematic of the capacitive switch bank composed of N capacitive switches. (b) Schematic of the varactor.

SEMICONDUCTOR BASED CAPACITIVE SWITCH BANK

A capacitive switch can be composed by a series connection of a fixed capacitor with a semiconductor based

switch (Fig. 2). When using (multiple stacked) diodes or transistors for the switching element, typically its behavior can be approximated by a resistor (R_{on}) in the ON state and a capacitor (C_{off}) in its OFF state. In order to achieve sufficient capacitance tuning range, the fixed capacitor C_{on} must be significantly larger than the off-state capacitance (C_{off}).

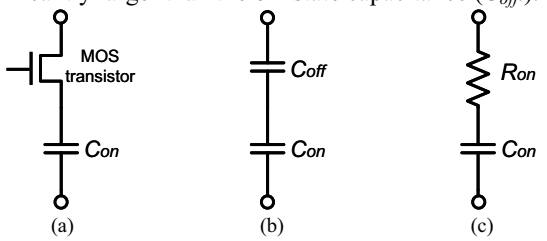

Fig. 2. (a) Schematic of a capacitive switch composed by a series connection of a fixed capacitor (C_{on}) with a MOS transistor. (b) Equivalent circuit of the capacitive switch in the OFF state. (c) Equivalent circuit of the capacitive switch in the ON state.

Since semiconductor based capacitive switches can provide a large capacitance density, it is relatively easy to integrate a large number of capacitive switches to achieve a fine tuning resolution. However, there is a stringent tradeoff between the tuning range and quality factor for a semiconductor based capacitive switch. To understand this, we consider Fig. 2. The best operation of such a capacitive switch is achieved when both R_{on} and C_{off} are small, yielding higher quality factor and capacitance tuning range. Note that lowering R_{on} through up-scaling of the switching device will typically increase the OFF-state capacitance (C_{off}), which in turn limits the resulting capacitance ratio (T_{tune}). In view of this, care is normally taken to improve the R_{on}-C_{off} product of the switching device by special process technologies, e.g. silicon-on-sapphire (SOS) CMOS [1] and pseudomorphic high-electron mobility transistors (pHEMT) [2]. Table I provides an overview of the current state-of-the-art R_{on}-C_{off} products of semiconductor based capacitive switches and their related $Q(T_{tune}$ -1) product, which can be found as

$$Q \cdot (T_{tune} - 1) = \frac{1}{\omega R_{on} C_{off}} \tag{1}$$

where ω is the angular RF frequency and

$$Q = 1/\left(\omega R_{on} C_{on}\right) \tag{2}$$

represents the quality factor of the capacitive switch in the ON state, while

$$T_{tune} = C_{on} / \left(\frac{C_{on} C_{off}}{C_{on} + C_{off}} \right) = 1 + \frac{C_{on}}{C_{off}} \tag{3}$$

is the capacitance ratio between ON and OFF states. Closer inspection of Table I indicates that the room for compromising between the quality factor and tuning range is in fact very limited, especially at RF frequencies. This clearly highlights the current bottleneck for semiconductor based capacitive switches. Consequently, their applications are mostly found below 2 GHz. In addition, note that when fine tuning of the capacitive device is needed, performance degradation due to the parasitics of the connecting network to the switch array will take place. Furthermore, the linearity of the semiconductor based capacitive switch bank is also a concern and challenge in their application.

TABLE I
SURVEY OF STATE-OF-THE-ART RON-COFF PRODUCTS FROM DIFFERENT PROCESS TECHNOLOGY AND CORRESPONDING Q-TTUNE PRODUCTS AT 2 GHZ AND 5 GHZ

Process Technology	$R_{on} \cdot C_{off}$ (fs)	$Q \cdot (T_{tune} - 1)$ at 2 GHz	$Q \cdot (T_{tune} - 1)$ at 5 GHz
0.5 μm 10 nm T_{ox} SOS	756 [1]	105	42
0.25 μm 5 nm T_{ox} SOS	448 [1]	178	71
0.5 μm pHEMT	360 [2]	221	88
0.15 μm pHEMT	435 [2]	183	73

CONVENTIONAL SEMICONDUCTOR VARACTORS

Semiconductor based varactors, like the p-n diode, Schottky diode and MOS varactors, are basically voltage-controlled capacitances, which provide continuously tuning making use of the voltage-dependent depletion layer thickness of the space charge region. Due to the relatively high dielectric constants of semiconductor materials, capacitance densities are typically at least 10 times larger than their MEMS counterparts. In addition, semiconductor based solutions have advantages in terms of integration, reliability, tuning speed (1-100 ns), low-control voltage and ruggedness. However, their inherently nonlinear behavior and low quality factor at microwave frequencies are considered to be incompatible with the requirements of modern wireless communication systems, which require high linearity and good quality factors.

SEMICONDUCTOR BASED LOW-DISTORTION VARACTORS

As mentioned above, for conventional semiconductor based varactors, tradeoffs are normally made between capacitance tuning range and linearity. This can be intuitively understood as follows. For a single varactor diode, increasing the tuning range for a constant breakdown voltage will yield bigger capacitance changes for an applied RF voltage, consequently its linearity will degrade. To overcome this conflict, recently several specific varactor diode topologies have been developed and implemented [3]-[11]. These proposed varactor configurations act as variable capacitors between their RF terminals with ideally zero, or extremely low distortion, while a third terminal is used for a "low-frequency" control voltage. A brief description of these low-distortion varactor configurations is given below.

- The distortion-free varactor stack (DFVS) [4], [6] is based on an anti-series connection of two identical uniformly doped diodes [Fig. 3(a)]. This uniform doping results in a capacitance power law coefficient of $n=0.5$ [12]. Furthermore, an "infinitely" high impedance is used

to connect to the center-tap of the diode configuration. Under these conditions, all distortion components at the RF terminals are perfectly cancelled, yielding a distortion-free operation.

- The high-tuning range varactor stack (HTRVS) [4] is a combined anti-series/anti-parallel topology of four hyperabrupt varactor diodes [Fig. 3(b)] [12]. Now a capacitance power law coefficient $n>0.5$ is applied along with two infinitely high center-tap impedances. At the RF terminals, the resulting even and third-order distortion products are cancelled through a proper selection of the varactor area ratio (X)

$$X = \frac{4n+1+\sqrt{12n^2-3}}{2(n+1)} \tag{4}$$

- The narrow tone-spacing varactor stack (NTSVS) [7]-[10] is based on an anti-series connection of two N_dx^{-2} doped diodes [Fig. 3(a)]. Note that this special doping profile results in exponential $C(V_R)$ behavior under reverse bias V_R. To cancel the third-order intermodulation distortion (IM_3), there must be a *low impedance* path (relative to the AC impedance of the varactor capacitance itself) between the center node (V_R) and the two RF terminals at low frequencies. At the same time, the high-frequency components (fundamental and higher harmonics) at the center tap node should experience high impedance, i.e., $Z_c(s)$ should be much larger than the AC impedance of the varactor diode itself at these frequencies. When these conditions are met, the IM_3 will be cancelled and the remaining distortion is dominated by the much smaller fifth-order nonlinearity.
- The wide tone-spacing varactor stack (WTSVS) [8] is a combined anti-series/anti-parallel topology of four N_dx^{-2} doped diodes, which uses an "infinitely" high impedance as center-tap connection [Fig. 3(b)]. This situation can be regarded as a special case of the HTRVS in which the capacitance power law coefficient n approaches infinity. This yields a corresponding varactor area ratio for IM_3 cancelation of $2\pm\sqrt{3}$. Note that this configuration shares the same doping profile as the NTSVS and therefore both configurations (WTSVS and NTSVS) can be implemented on the same wafer while offering complementary linearity properties in terms of tone spacing.

Although the different varactor configurations discussed above, all provide for the given conditions a voltage-controlled tunable capacitance, they do differ in their implementation, and their linearity properties versus modulation bandwidth. In summary, the varactor configurations that use infinitely high center-tap impedance(s) (i.e., DFVS, HTRVS and WTSVS) provide the best linearity for signals that have a relatively large frequency spacing (several hundred kilohertz). This property makes these configurations most suited for (adaptive) receiver applications where cross modulation of the "weak" desired signals by strong out-of-band interferers should be avoided. In (adaptive) transmitting systems, however, the in-band linearity will be the biggest concern. For these applications the NTSVS [7] is recommended, since it provides the highest linearity for in-band signals (up to ten's of MHz's). Moreover, the fact that this latter configuration makes use of a base-band "short" (typically an inductor) for the connection to the varactor stack center tap, facilitates rapid modulation of its tunable capacitance, something that is beneficial for future RF applications like dynamic load-line power amplifiers or modulators. As far as integration is concerned, the WTSVS can be easily integrated with the NTSVS since they can share the same doping profile. Therefore the different linearity requirements of both transmit and receive chains can be addressed in one single technology.

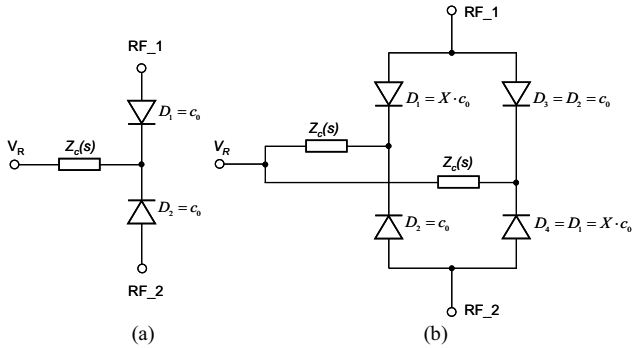

Fig. 3. (a) Anti-series configuration for DFVS and NTSVS. (b) Anti-series/anti-parallel configuration for HTRVS and WTSVS. $Z_c(s)$ is used to achieve specific harmonic termination conditions.

A) Doping Profile Considerations

In order to achieve the capacitance power law coefficient (n) of 0.5 for the DFVS, a uniform doping profile is required as shown Fig. 4(a). This doping concentration needs to be chosen carefully since this sets the quality factor and device breakdown. When the desired tuning range ($T_{tune} = C_{max}/C_{min}$ where C_{max} and C_{min} are the maximum and minimum capacitance values, respectively) is known, together with the material parameters, like maximum electric field ($E_{breakdown}$), dielectric constant (ε_s), mobility (μ_n) and built-in potential (V_j), the best choice for the doping concentration ($N_{uniform}$) can be selected using [11]

$$N_{uniform} = \frac{\varepsilon_s E^2_{breakdown}}{2eV_j(T^2_{tune}-1)}. \tag{5}$$

where e is the electron charge. With this selection, the related highest achievable intrinsic quality factor for the varactor at zero bias (Q_{opt}) operation is defined as

$$Q_{uniform}\Big|_{V_R=0} = \frac{\mu_n E^2_{breakdown}}{2\omega V_j(T^2_{tune}-1)(T_{tune}-1)}, \tag{6}$$

where ω is the angular RF frequency.

For the NTSVS and WTSVS, the required N_dx^{-2} doping profile, which provides the exponential $C(V_R)$ relationship, is shown in Fig. 4(b). Since we cannot implement infinitely

high or extremely low doping concentrations, the $N_d x^{-2}$ relationship is restricted between x_{low} and x_{high}, which automatically defines the useful capacitance tuning range. To maintain the "exponential" $C(V_R)$ relation and avoid reduced breakdown voltage and quality factor, a lowly doped spacer layer [Region 1 in Fig. 4(b)] is required. In contrast to the uniformly doped case, here a free-to-choose combination of tuning range and maximum reverse applied voltage (V_{R_max}) can be selected, after which the intrinsic quality factor can be optimized by dimensioning the doping profile. The resulting doping profile and maximum achievable intrinsic quality factors at zero bias for these structures can be written as [7]

$$N(x) = \frac{\varepsilon_s V_{R\_\max}}{e \ln(T_{tune})} x^{-2}, \tag{7}$$

$$Q\big|_{V_R=0} = \frac{3\mu_n \ln(T_{tune})}{\omega V_{R\_\max}(T_{tune}^3 - 1)} \left(\frac{T_{tune} E_{breakdown}}{T_{tune} - 1} \right)^2. \tag{8}$$

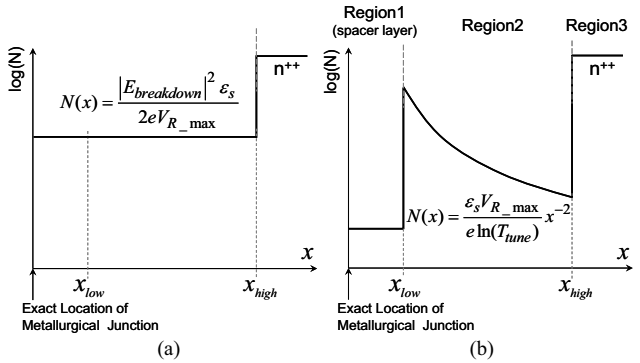

Fig. 4. (a) Optimized doping profile of the uniform doped diode for the DFVS. (b) Optimized doping profile for the NTSVS and WTSVS to achieve the exponential $C(V_R)$ relation.

B) Implementation of High-Q Varactors

In practice, the parasitics caused by the buried layer, metal interconnections, ohmic contacts and substrate, will degrade the quality factor of the intrinsic varactor.

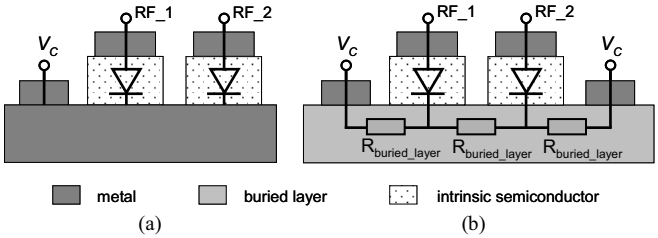

Fig. 5. (a) Cross section of a varactor stack implemented in SOG technology where thick metal interconnections may be placed on both sides of the intrinsic material. In the future, this can be applied to compound semiconductor technologies as well. (b) Cross section of a varactor stack implementation using the buried layer for backside interconnection of the varactors in non-substrate transfer technologies as conventional GaAs and SiC technologies.

For simplicity, all the losses of the parasitics can be attributed to a lumped parameter ($Q_{parasitics}$) and the resulting total quality factor (Q_{total}) can be expressed as

$$Q_{total} = \frac{Q_{intrinsic} Q_{parasitics}}{Q_{intrinsic} + Q_{parasitics}} \tag{9}$$

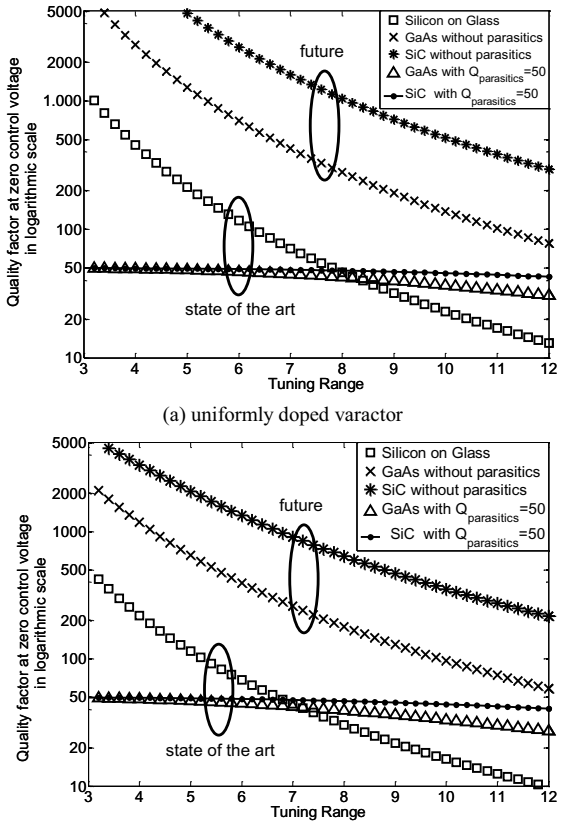

Fig. 6. Maximum achievable quality factor at zero bias for different technologies. (a) uniformly doped varactor with a built-in voltage of 0.7 V. (b) $N_d x^{-2}$ doped varactor with a maximum voltage of 15 V. (The frequency is 2 GHz.)

When the varactor stack is implemented with silicon-on-glass (SOG) technology [5] as shown in Fig. 5(a), the intrinsic varactor can be directly contacted by thick metal interconnects on both sides, and therefore the total quality factor will be determined by $Q_{intrinsic}$. It is important to note that the quality factor decreases rapidly with the increase of the tuning range due to the need of a thicker intrinsic material as indicated in (6) and (8). To circumvent this problem, compound semiconductors can be used to further improve the intrinsic quality factor, e.g. compared to silicon an enhancement factor of 6-8 is feasible when using a GaAs implementation, while a factor as large as 25 is possible for SiC. However, in GaAs or SiC technologies, as shown in Fig. 5(b), the use of a buried layer under the intrinsic area for interconnection is currently required for process compatibility, which raises parasitic losses and limits the overall quality factor to a certain degree. To study this limitation, in Fig. 6(a) and (b), the maximum achievable quality factors at zero bias are plotted as function of tuning range for the uniformly doped varactor and $N_d x^{-2}$ doped varactor. It reveals that, at the current stage [see the curves

marked with "state of the art" in Fig. 6(a)], the silicon-on-glass (SOG) technology provides a superior quality factor when the tuning range is moderate (e.g. less than 6:1), while much better results can be achieved with conventional GaAs and SiC technologies for varactors with large tuning ranges (currently the typical value for $Q_{parasitic}$ is around 50). In the future, with the elimination of parasitics in compound semiconductor technologies (e.g. through the use of backside contacts in the GaAs or SiC technologies), superior quality factors beyond what are needed for mobile communications can be expected [see the curves marked with "future" in Fig. 6(b)].

The performance of the implemented DFVS, NTSVS and WTSVS [6], [8], [10] are listed in Table II. It reveals that the realized semiconductor based ultra low-distortion varactor circuits [6], [8], [10] achieve state-of-the-art performance for tuning range, linearity, and quality factor when compared against all existing technology platforms for continuously tunable elements.

TABLE II
PERFORMANCE COMPARISON OF CONTINUOUSLY TUNABLE VARACTORS

Technology	Tuning range	Average Q factor	Control voltage	OIP_3 (dBm)
ferroelectric BST (1.3 GHz) [13]	2:1	30-35	-10 V-10 V	35-50
MEMS (1 GHz) [14]	~ 1.4:1	N.A.	0 V-2.5 V	~ 40
MEMS (40 GHz) [15]	4:1	> 80	20 V- 34 V	N.A.
Conventional Semiconductor SiC (2 GHz) [16]	5.6:1	20-30	0 V-15 V	N.A.
SOG DFVS (2 GHz) [6]	3.3:1	100-300	0 V-10 V	~ 60
SOG NTSVS and WTSVS (2 GHz) [8]	3.5:1	80-100	0 V-12 V	~ 60
GaAs NTSVS (2 GHz) [10]	9:1	~ 50	0 V-15 V	57

CONCLUSIONS

In this paper, the semiconductor based tunable RF components are reviewed for their performance. Benefits and shortcomings are discussed yielding the conclusion that the recently proposed ultra low-distortion semiconductor based varactor configurations can provide state-of-the-art performance in terms of tuning range, linearity, quality factor, control voltage, capacitance density, reliability and technology compatibility in combination with low packaging costs. Although the current implementation of NTSVS using GaAs has not been optimized for quality factor, the measured results already represent the current state-of-the-art in tuning range, linearity and quality factor among all existing continuously tunable elements. It is predicted that, with the elimination of parasitics in compound semiconductor technologies, by backside processing and contacting, in the future, close to ideal tunable RF components can be realized, representing a significant opportunity for compound semiconductors.

ACKNOWLEDGEMENTS

The authors acknowledge Skyworks Solutions, Inc., Newbury Park, CA, USA, NXP Semiconductors, the Netherlands, and the PANAMA and MEMPHIS projects for their support.

REFERENCES

[1] D. Kelly, et al., "The state-of-the-art of silicon-on-sapphire CMOS RF switches," CSIC 2005 digest, pp. 200-203, Nov. 2005.
[2] S. Makioka, et al., "Super self-aligned GaAs RF switch IC with 0.25 dB extremely low insertion loss for mobile communication systems," *IEEE Trans. Electron Devices*, vol. 48, pp. 1510-1514, Aug. 2001.
[3] R. G. Meyer and M. L. Stephens, "Distortion in variable-capacitance diodes," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 47-55, Feb. 1975.
[4] K. Buisman, et al., "'Distortion-free' varactor diode topologies for RF adaptivity," *IEEE MTT-S Int. Microwave Symposium Dig.*, pp. 157-160, 2005.
[5] K. Buisman, et al., "A monolithic low-distortion low-loss silicon-on-glass varactor-tuned filter with optimized biasing," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 11, pp. 749-751, Nov. 2006.
[6] K. Buisman, et al., "Varactor topologies for RF adaptivity with improved power handling and linearity," *IEEE MTT-S Int. Microwave Symposium Dig.*, pp. 319-322, 2007.
[7] C. Huang, et al., "Enabling low-distortion varactors for adaptive transmitters," *IEEE Trans. Microwave Theory Tech.*, vol. 56, pp. 1149-1163, May. 2008.
[8] C. Huang, et al., "Ultra linear low-loss varactor diode configurations for adaptive RF systems," *IEEE Trans. Microwave Theory Tech.*, to be published in Jan. 2009.
[9] C. Huang, et al., "A 67 dBm OIP_3 multi-stacked junction varactor," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 11, pp. 749-751, Nov. 2008.
[10] C. Huang, et al., "A GaAs Junction Varactor with a Continuously Tunable Range of 9:1 and an OIP_3 of 57 dBm," *IEEE Electron Device Letter,* vol. 31, no. 2, pp. 108-110, Feb. 2010.
[11] L. K. Nanver, et al., "Improved RF Devices for Future Adaptive Wireless Systems Using Two-sided Contacting and AlN Cooling", *IEEE J. Solid-State Circuits*, vol. 44, no. 9, Sep. 2009.
[12] D. A. Neamen, "Semiconductor Physics & Devices", 2nd ed., Chicago: Irwin, 1997.
[13] J. S. Fu, et al., "A linearity improvement technique for thin-film barium strontium titanate capacitors," in *IEEE MTT-S Int. Microwave Symp. Dig.,* San Francisco, CA, pp. 560-563, Jun. 2006.
[14] D. Girbau, et al., "Study of intermodulation in RF MEMS variable capacitors," *IEEE Trans. Microwave Theory Tech.*, vol. 54, pp. 1120-1130, Mar. 2006.
[15] D. Peroulis and L. P. B. Katehi, "Electrostatically-tunable analog RF MEMS varactors with measured capacitance range of 300%," *IEEE MTT-S Int. Microwave Symp. Dig.,* vol. 3, pp. 1793-1796, Jun. 2003.
[16] M. Sudow, et al., "SiC varactors for dynamic load modulation of high power amplifiers," *IEEE Electron Device Lett.,* vol. 29, no. 7, pp. 728-730, Jul. 2008.

ACRONYMS

DFVS: Distortion-Free Varactor Stack
HTRVS: High Tuning Range Varactor Stack
NTSVS: Narrow Tone-Spacing Varactor Stack
WTSVS: Wide Tone-Spacing Varactor Stack
SOG: Silicon On Glass
BST: Barium Strontium Titanate
MEMS: Micro Electro-Mechanical System